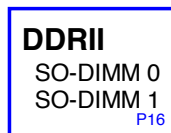
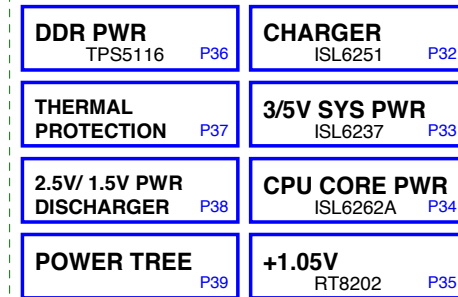
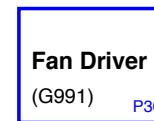
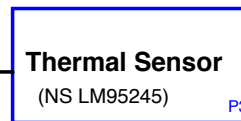
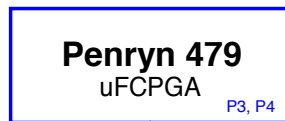
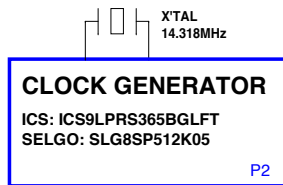
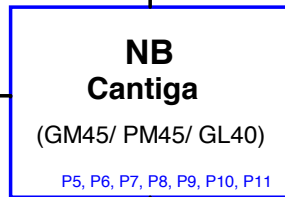


ZK2 SYSTEM BLOCK DIAGRAM

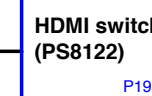
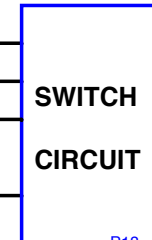
BOM MARK
 I@: INT VGA
 E@: STUFF FOR EXT VGA
 ND@: STUFF FOR NON-DOCK
 D@: DOCK
 SP@: SPECIAL FOR EXT/INT VGA



Dual Channel DDR2
 667/800 MHz

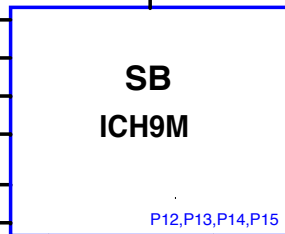
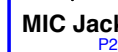
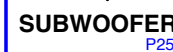
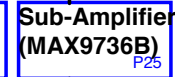
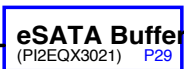
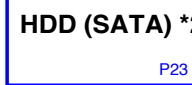


EXT_LVDS
 EXT_CRT
 EXT_DVI
 INT_LVDS
 INT_CRT



MP-Stage

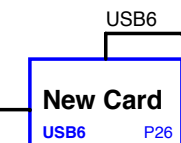
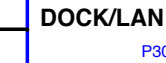
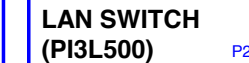
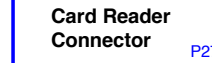
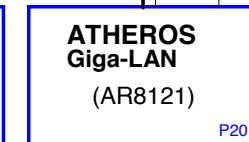
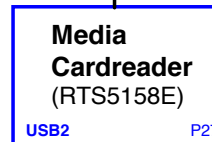
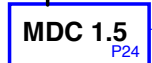
31ZK2MB0000: ZK2 MB ASSY(GM/UMA)ASSY W/O CPU
 31ZK2MB0010: ZK2 MB ASSY(PM/MXM)ASSY W/O CPU
 31ZK2MB0020: ZK2 MB ASSY(PM/MXM) W/O CPU/E-SATA



SATA0
 SATA4
 SATA1
 SATA5
 USB 2.0
 Azalia

SPI

LPC



USB6

USB2 & 3

PCI-Express

PCI-E-1

PCI-E-2&4

PCI-E-6

USB8

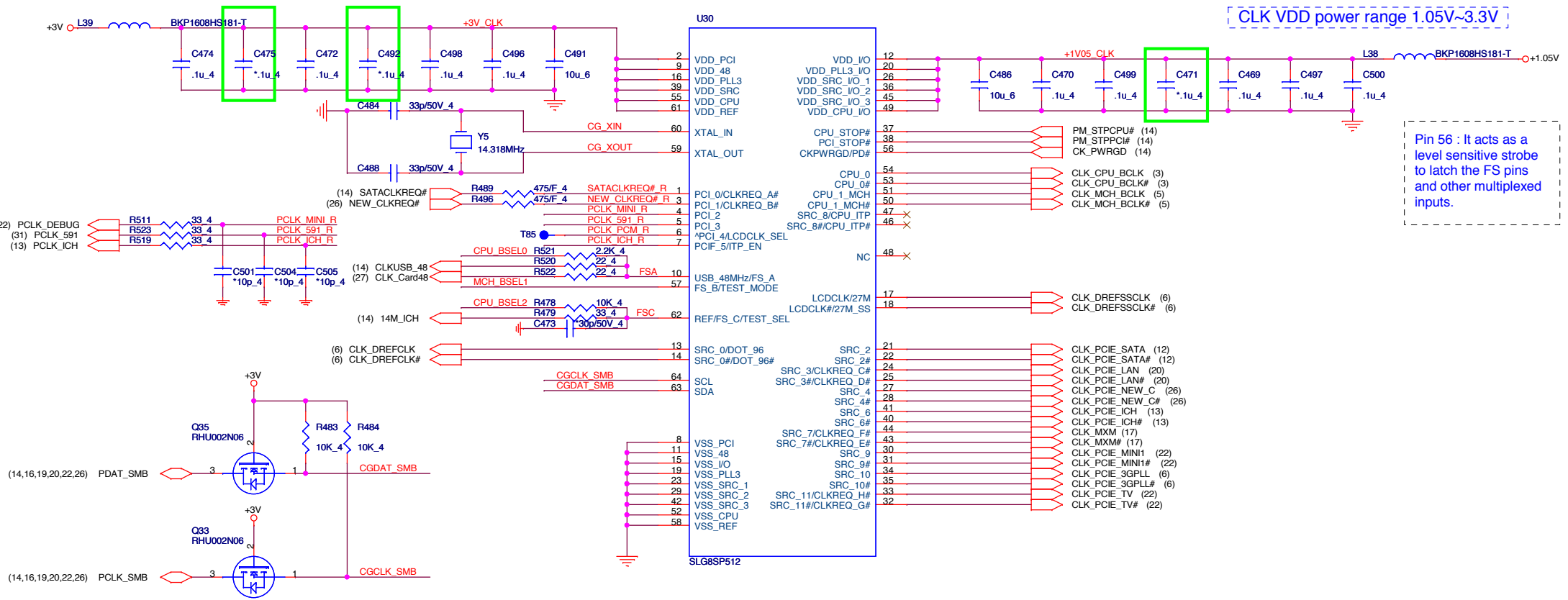
X'TAL 32.768KHz

X'TAL 25MHz

DA0ZK2MB6D0
 DA0ZK2MB6C0
 DA0ZK2MB6B0
 DA0ZK2MB6A0

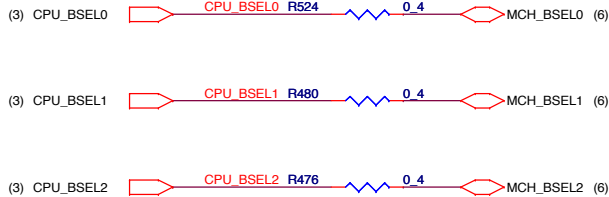
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Clock Generator



CPU Clock select

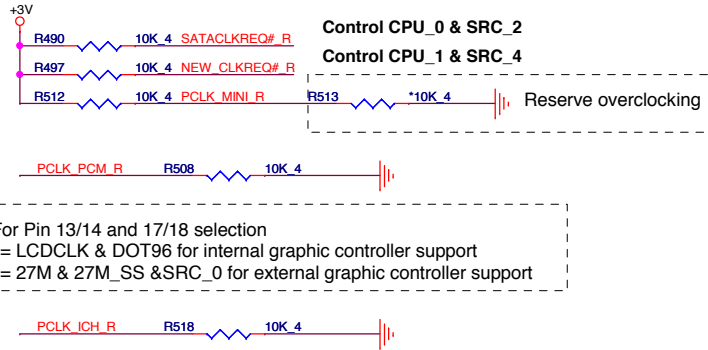
Pin 10/57/62 : For Pin CPU frequency selection



BSEL Frequency Select Table

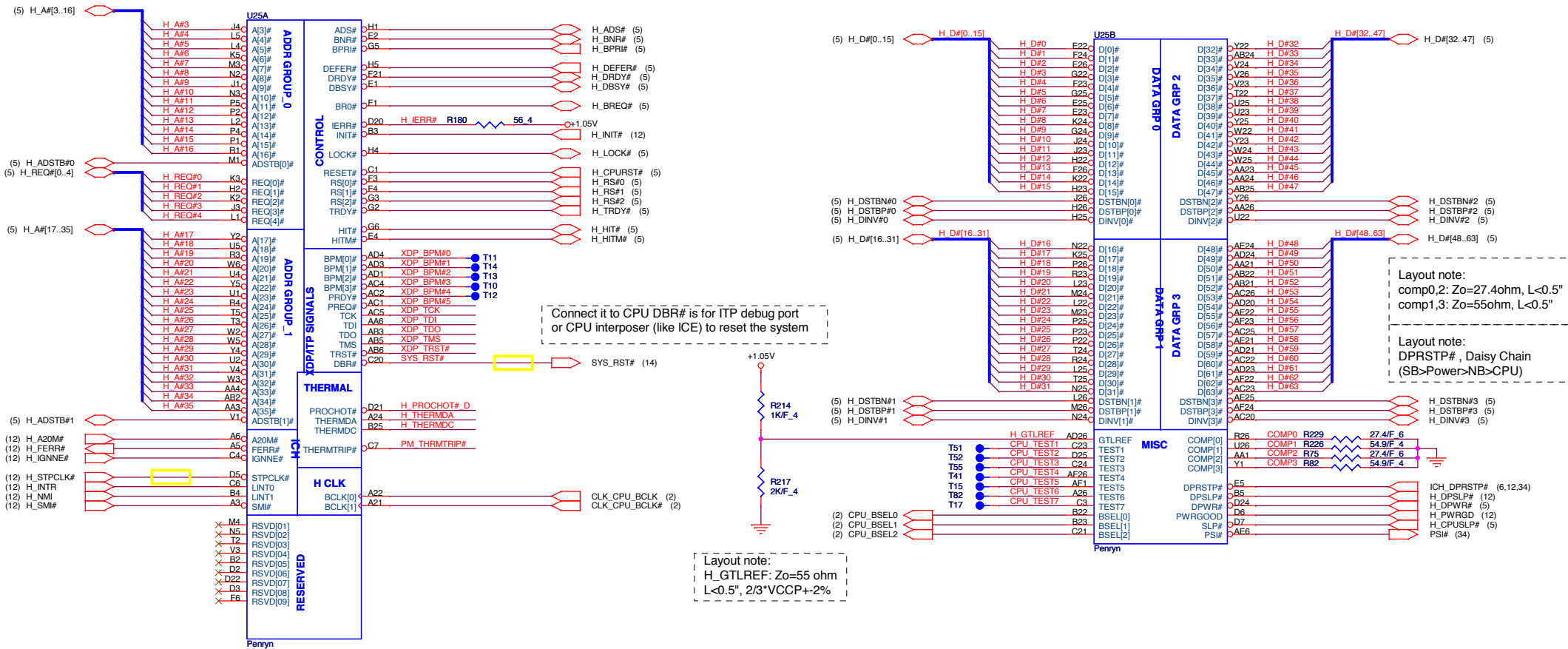
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

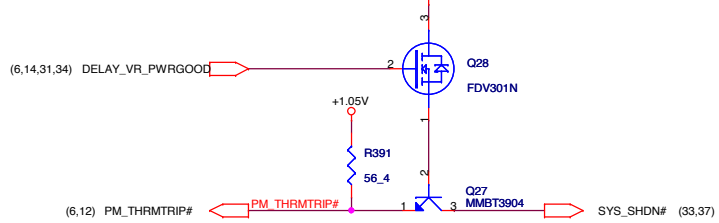


Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS & SRC_0 for external graphic controller support

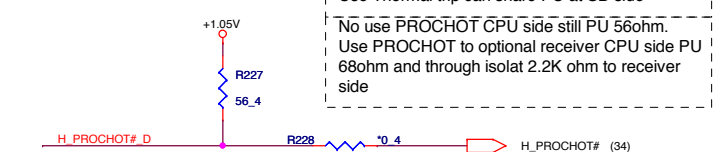
Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8



Thermal Trip

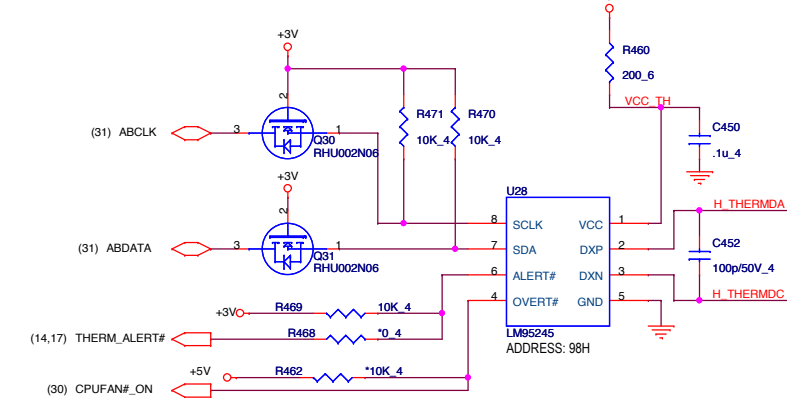


Processor hot

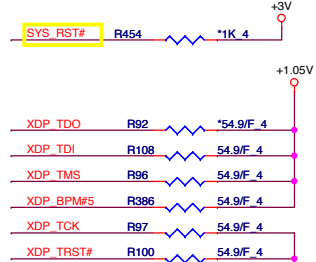


CPU 1/2

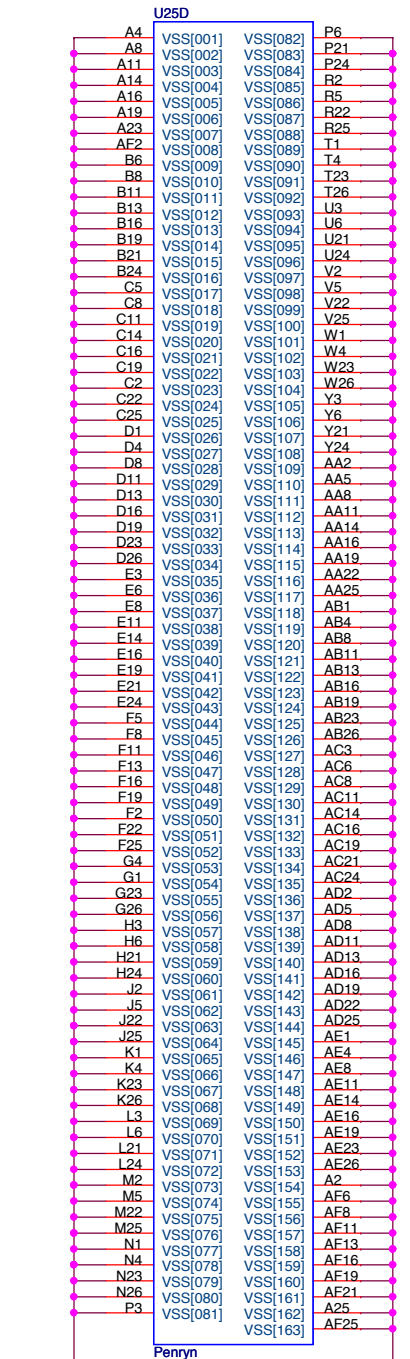
CPU Thermal Dbr monitor



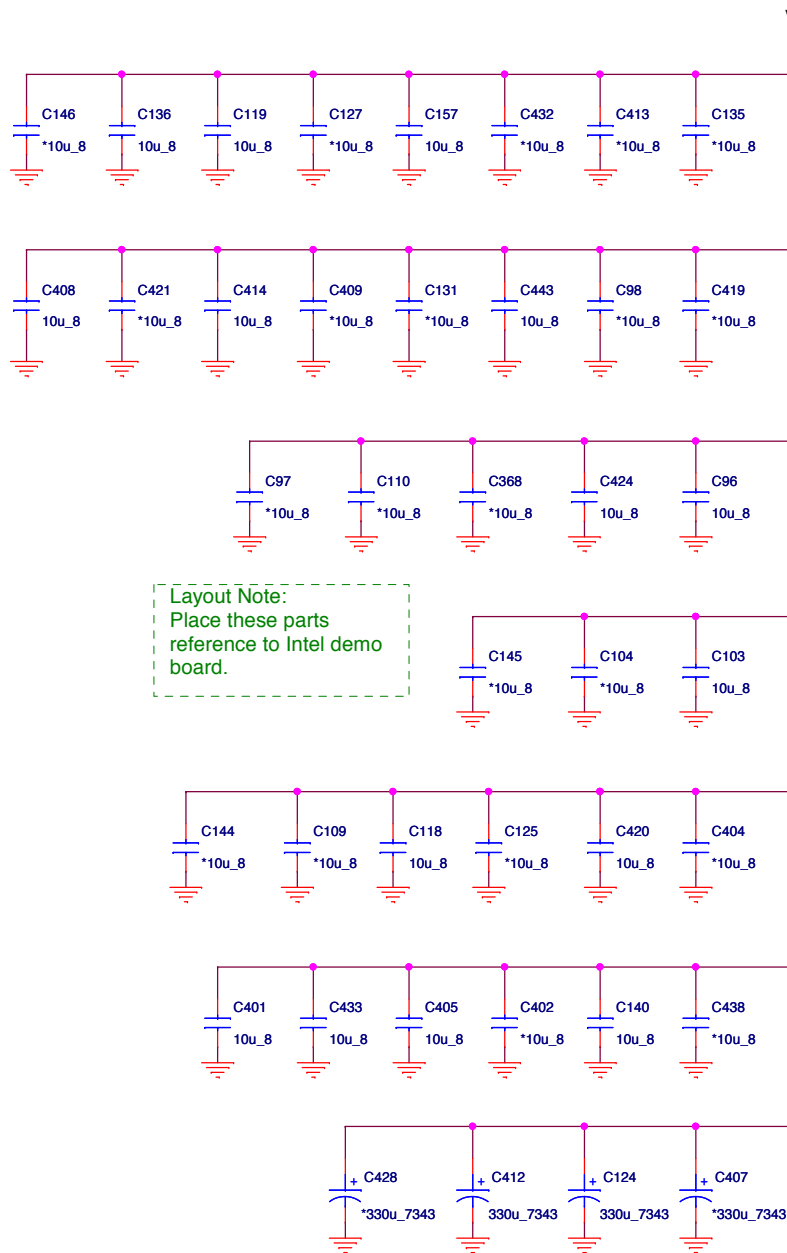
XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP



CPU 2/2

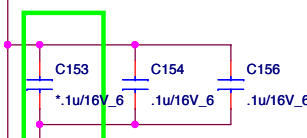
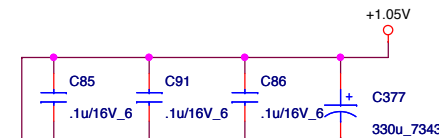


Layout Note:
Place these parts
reference to Intel demo
board.

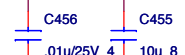
VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



VCCA:130mA +1.5V



R118 100/F_6 VCC_CORE

VCCSENSE (34)

VSSSENSE (34)

Layout Note:
Z0=27.4,P/U/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

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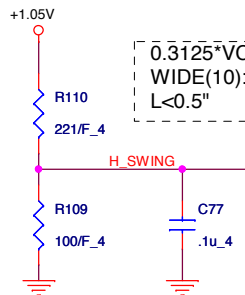
Quanta Computer Inc.

PROJECT : ZK2

CPU Power

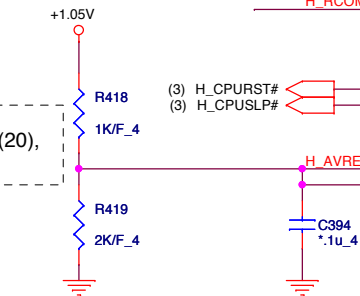
Size	Document Number	Rev 3B
Date: Tuesday, July 15, 2008	Sheet 4 of 39	

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06

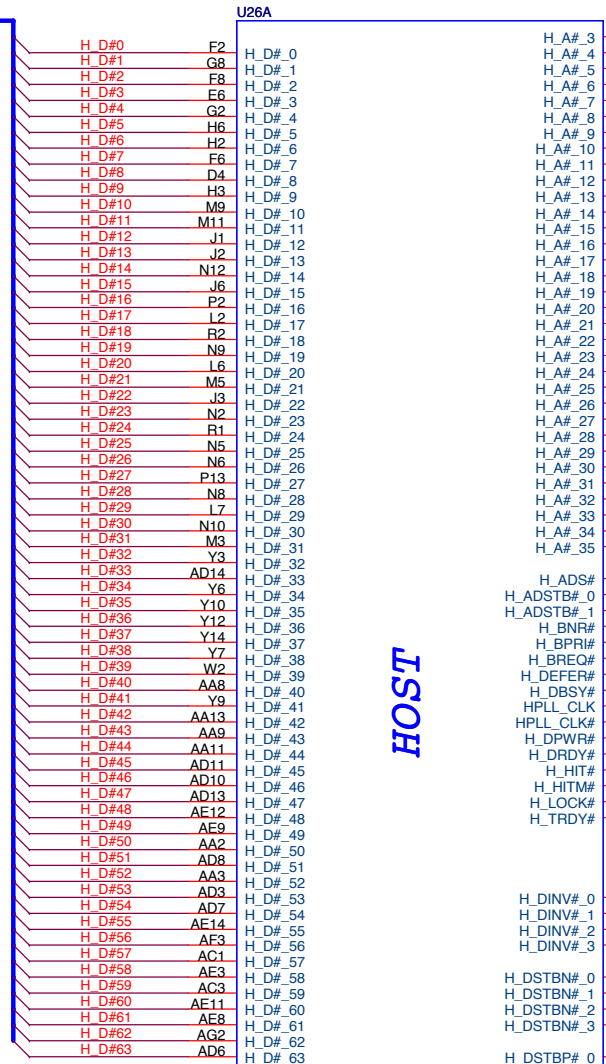


0.3125*VCCP
WIDE(10):SPACING(20),
L<0.5"

Layout Note:
WIDE(10):SPACING(20),
L<0.5"



2/3*VCCP
WIDE(10):SPACING(20),
L<0.5"



HOST

Quanta Computer Inc.
PROJECT : ZK2
GMCH HOST

Size	Document Number	Rev
		3B
Date:	Tuesday, July 15, 2008	Sheet 5 of 39

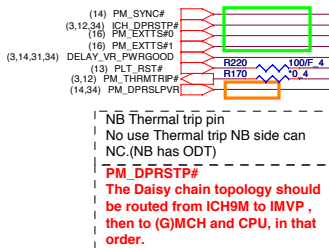
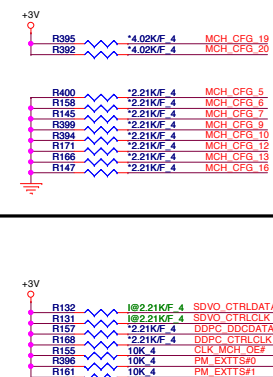
GMCH (CANTIGA)

www.vinafix.vn

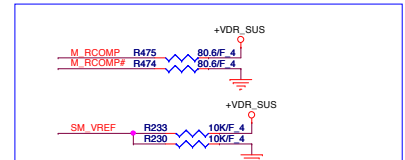
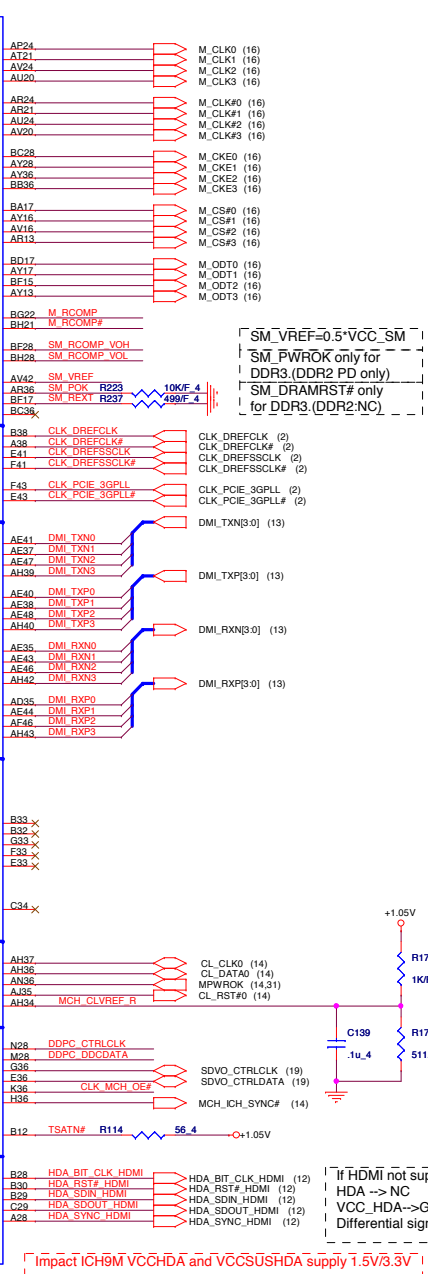
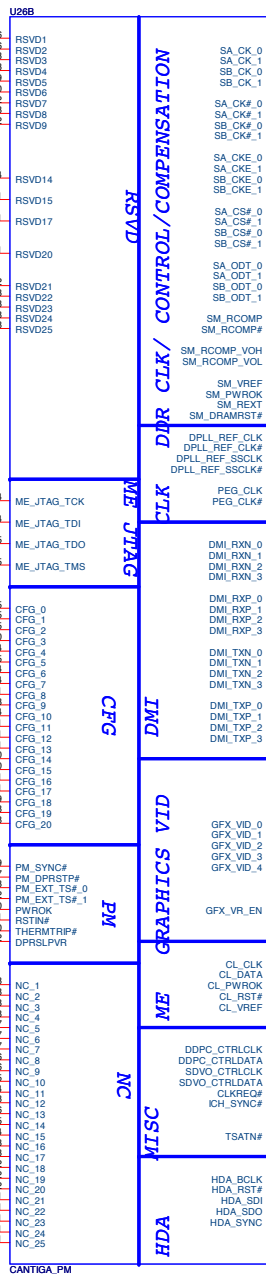
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin

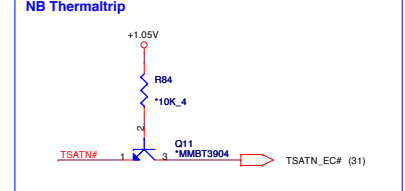
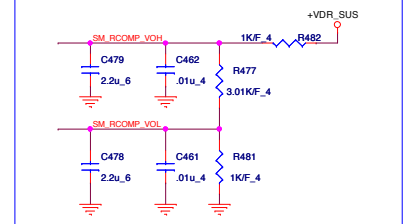


NB Thermal trip pin
No use Thermal trip NB side can NC (NB has ODT)
PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP, then to (G)MCH and CPU, in that order.



SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics



Check list note : CL_VREF=0.35V

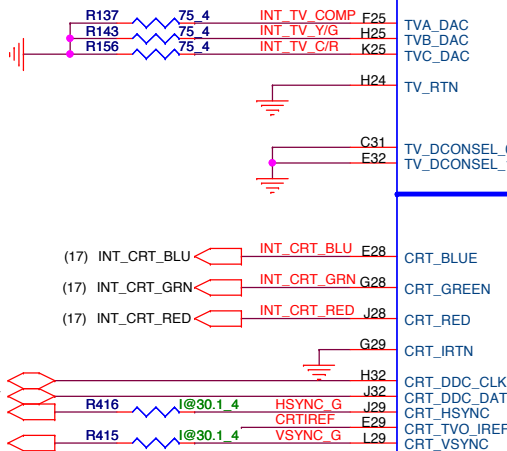
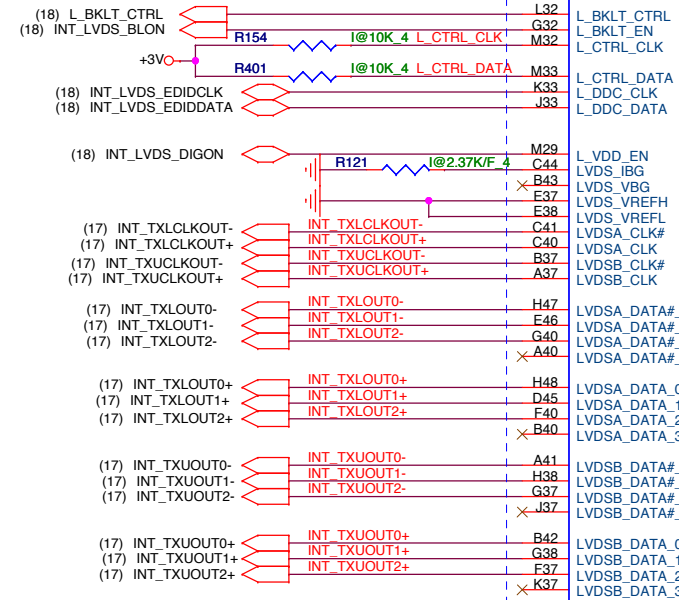
DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B
If TSATN# is not used, then it must be terminated with a 56- pull-up resistor to VCCP.
<Checklist ver0.8>
HDA -> NC
VCC_HDA->GND
Differential signal->NC
<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V
NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

IV@
EV@
SP@

IV&EV Dis/Enable setting

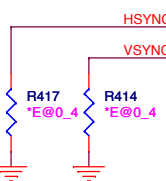
If LVDS no use, all signal can NC



HSYNC/VSYNC serial R place close to NB

CRTIREF pull down for IV cantiga 1.02k ohm/F

MXM STUFFED.



L<0.5", If PCIE not support still connect to +VCC_PEG

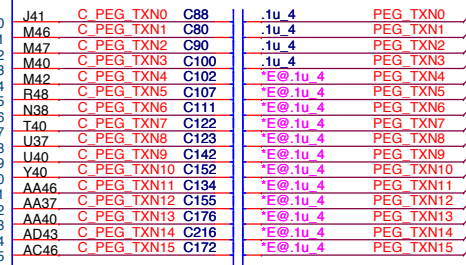
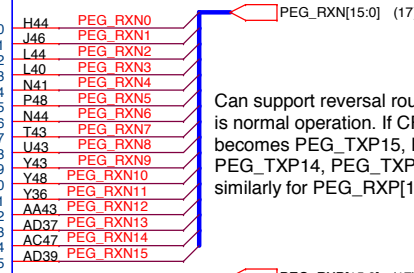
PEG_COMPI
PEG_COMPO

PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15

PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15

PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15



Can support reversal routing. If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a) For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC. What is correct.
b) For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC These signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>

For EV@

CRT R/G/B 0ohm to GND CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND CRTIREF 1.02Kohm to GND

<check list>

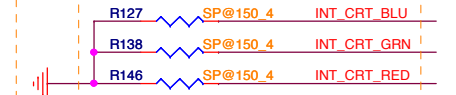
For IV@

CRTIREF
For IV: 1.02Kohm
For EV: 0ohm



SP@

CRT R/G/B
For IV: 150ohm
For EV: 0ohm



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PROJECT : ZK2

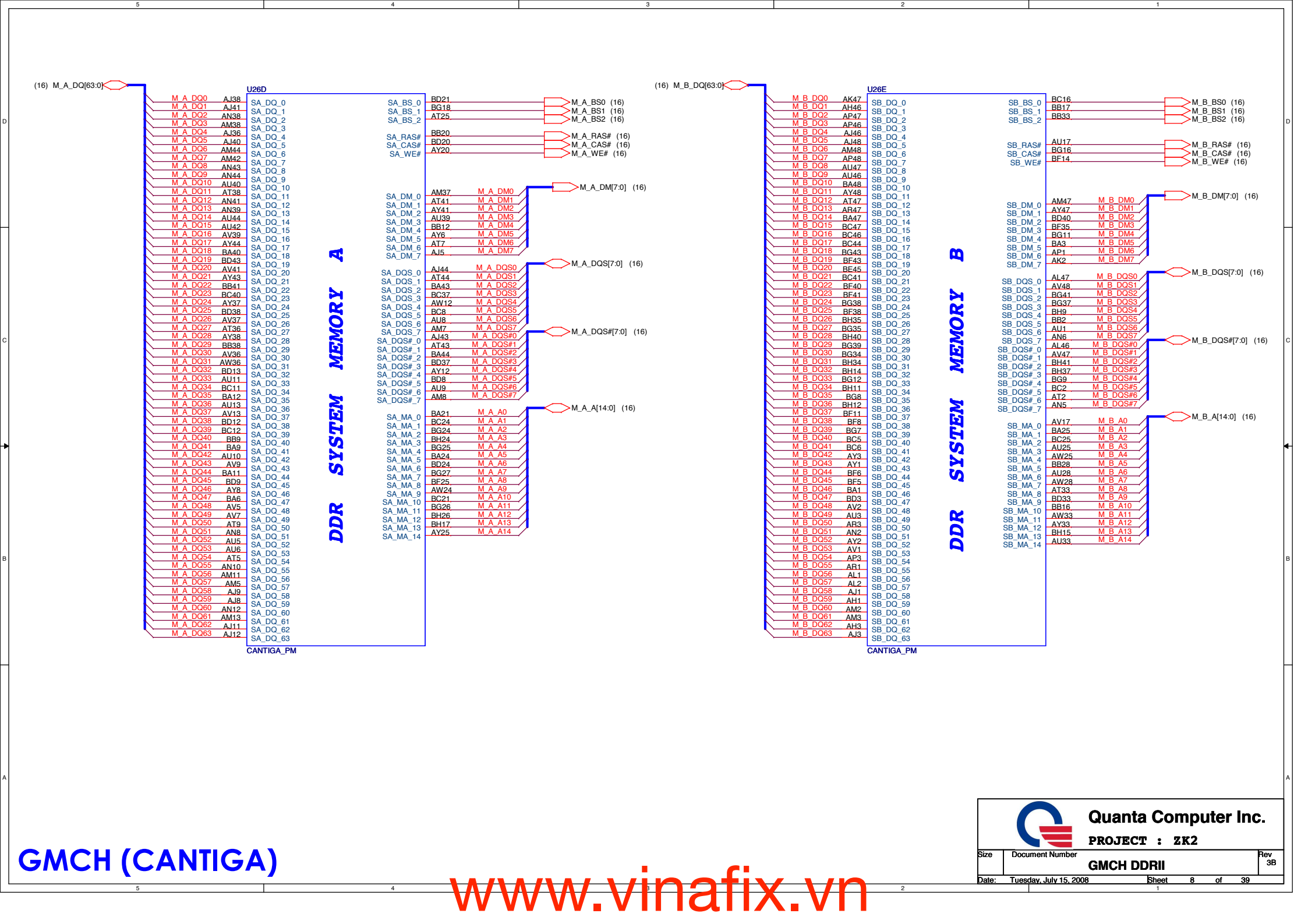
GMCH VGA

Size Document Number

Date: Tuesday, July 15, 2008

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Rev 3B



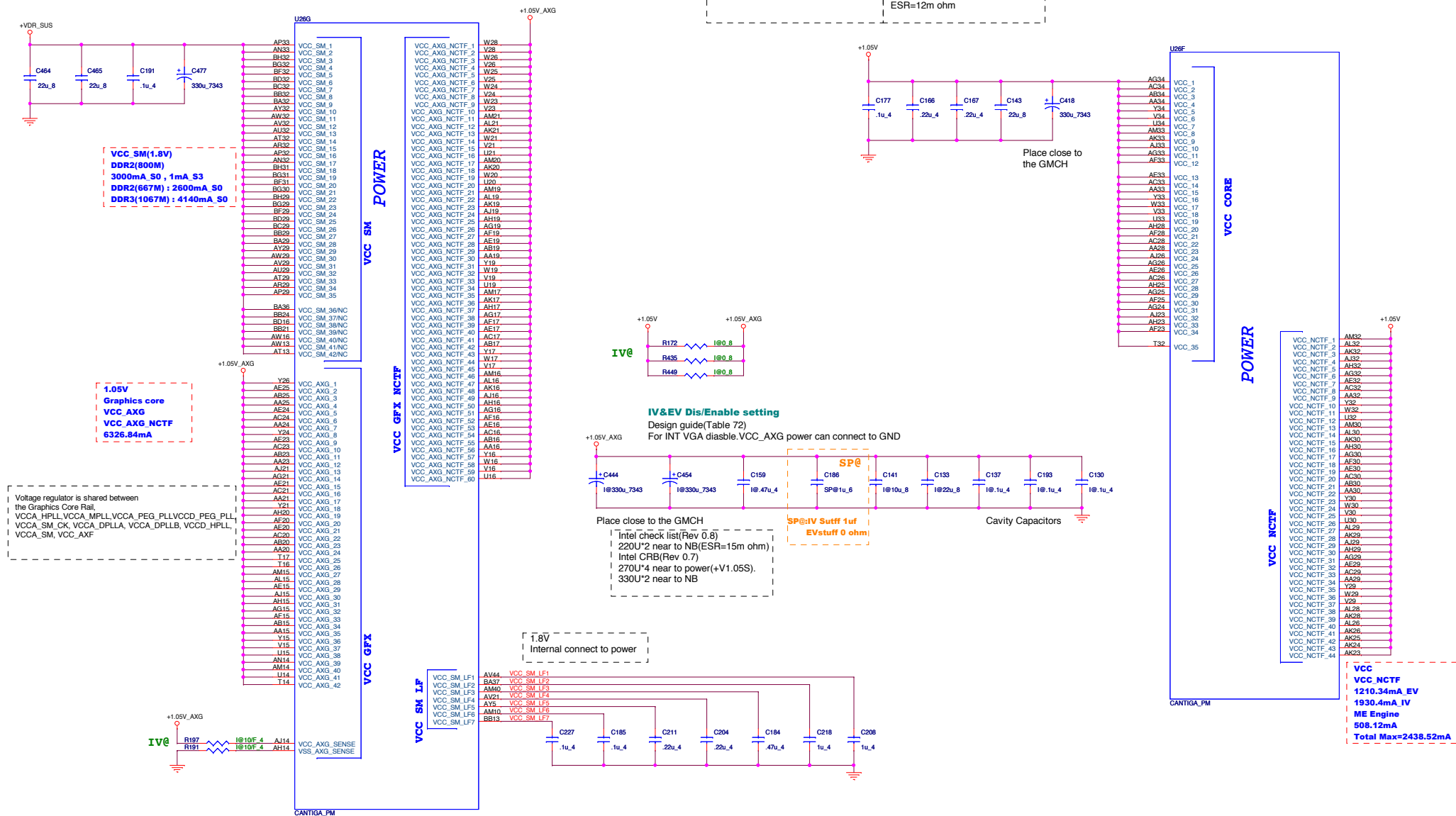
GM	TDP	10.5~12W
GS	TDP	7~8W
PM	TDP	7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

```

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESB=12m ohm

```



1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

GMCH (CANTIGA)

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VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

IV@
EV@
SP@

1210 100H, 10%
0.45A DCR_max = 0.39

1210 100H, 10%
0.45A DCR_max = 0.39

1210 0.1uH, 20%, 1A
DCR_max=0.078

3.3V
24.15mA for VCCA_TV_DAC
39.48mA for VCCA_TV_DAC
24.15mA for VCCA_TV_DAC
Total 87.78mA

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

VCCD_TV_DAC always keep 0.1U/0.022U/10U to +1.5V

1.5V
48.363mA for CRT
5mA for TV

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

FB 220 @100 MHz, 25%, 2A

ESR=60m ohm

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

USE same GND plane

CRB : 0 ohm
Check list : 2.2nH

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

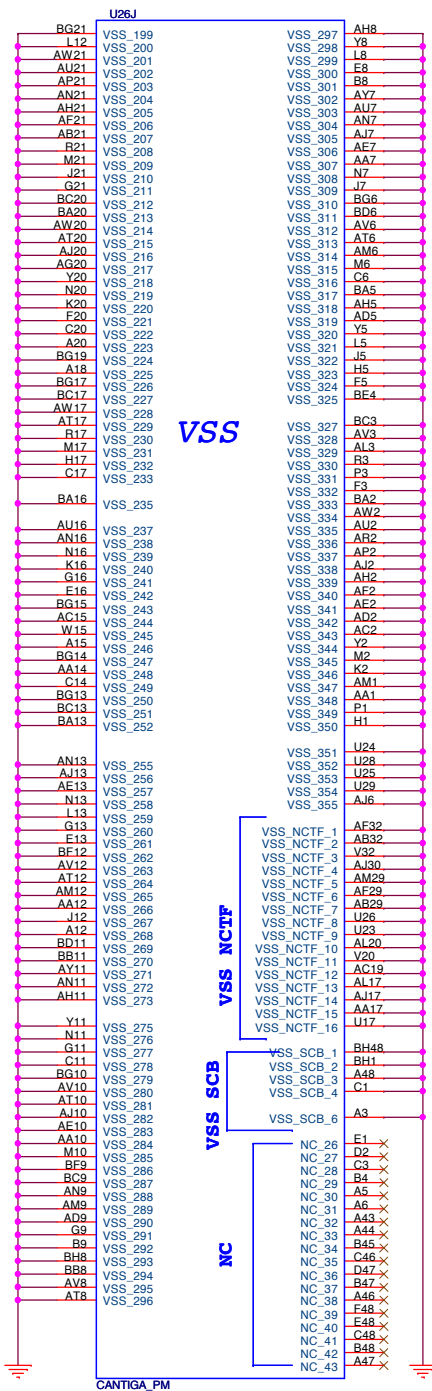
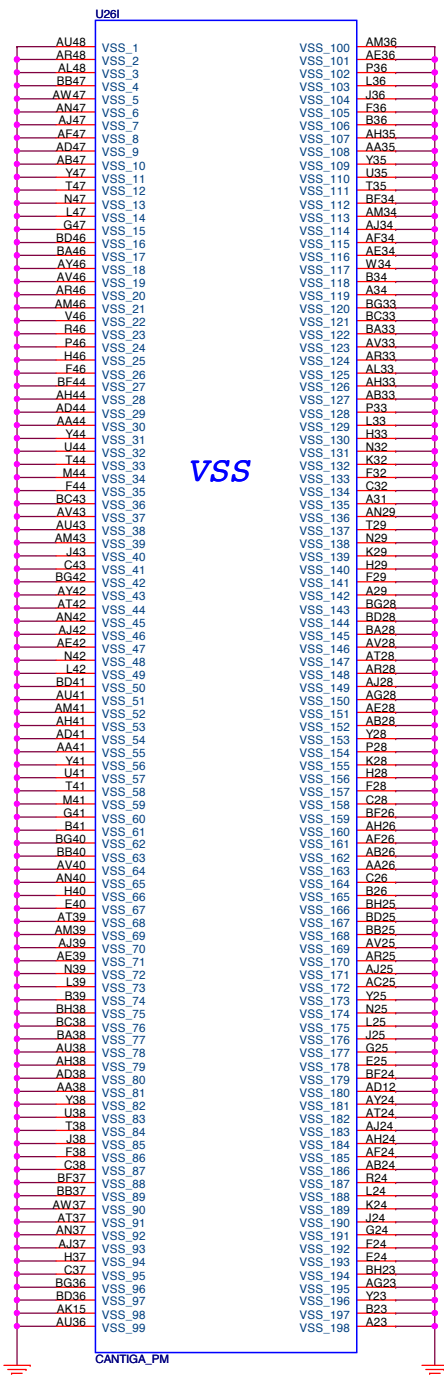
IV&EV Dis/Enable setting

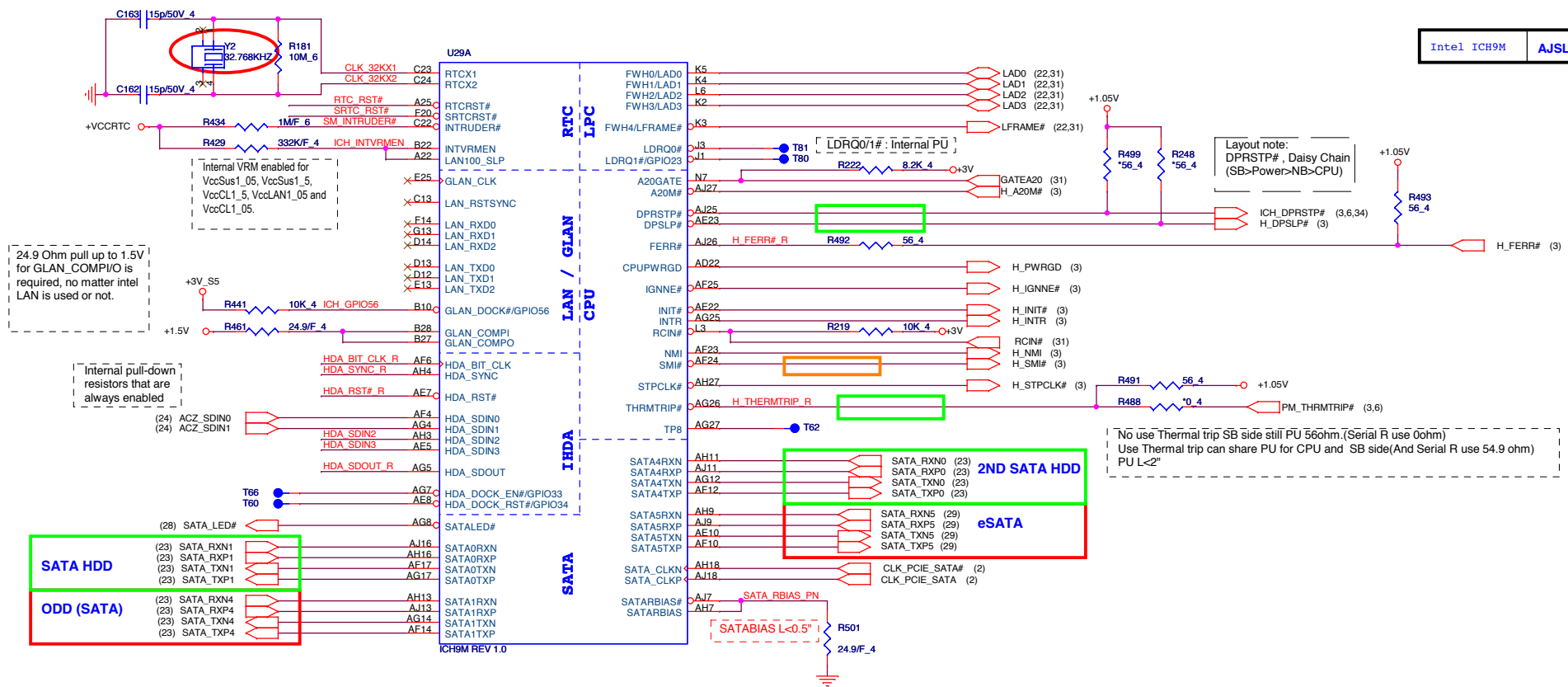
SP@:INT use 1 U
EXT use 0 ohm

SP@:INT use 0.01U
EXT use 0 ohm

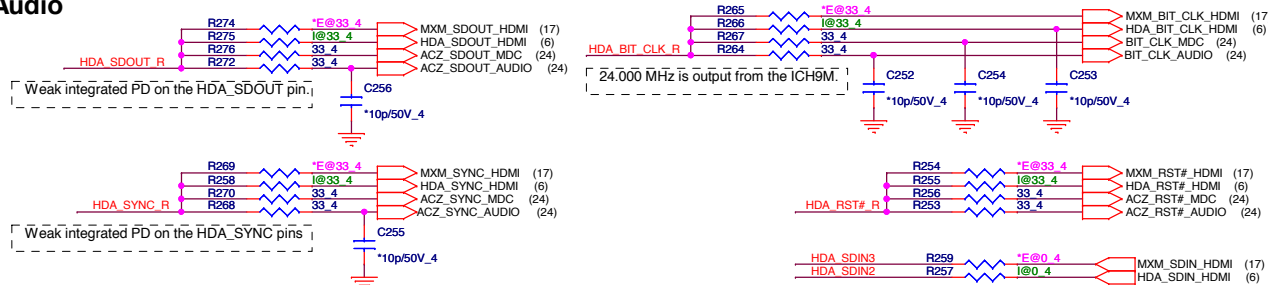
Power Net Name	Cantiga(V)
VCC_AXG_#	1.05V
VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCC_AXF_NCTF_#	1.05V
VCCA_PEG_PLL	1.05V

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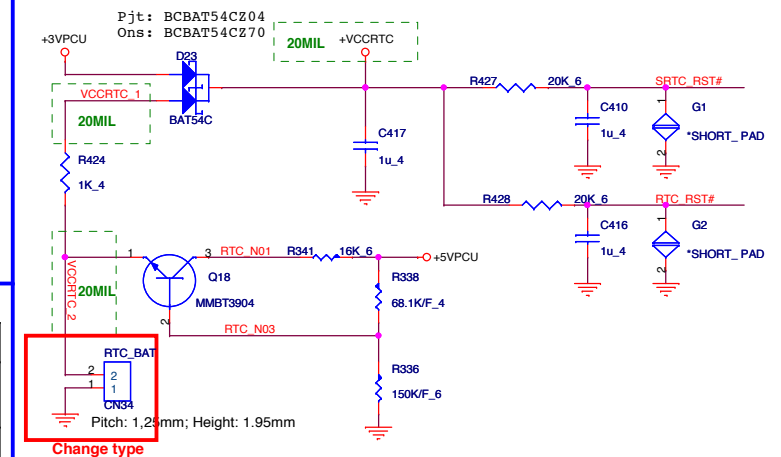




HD Audio

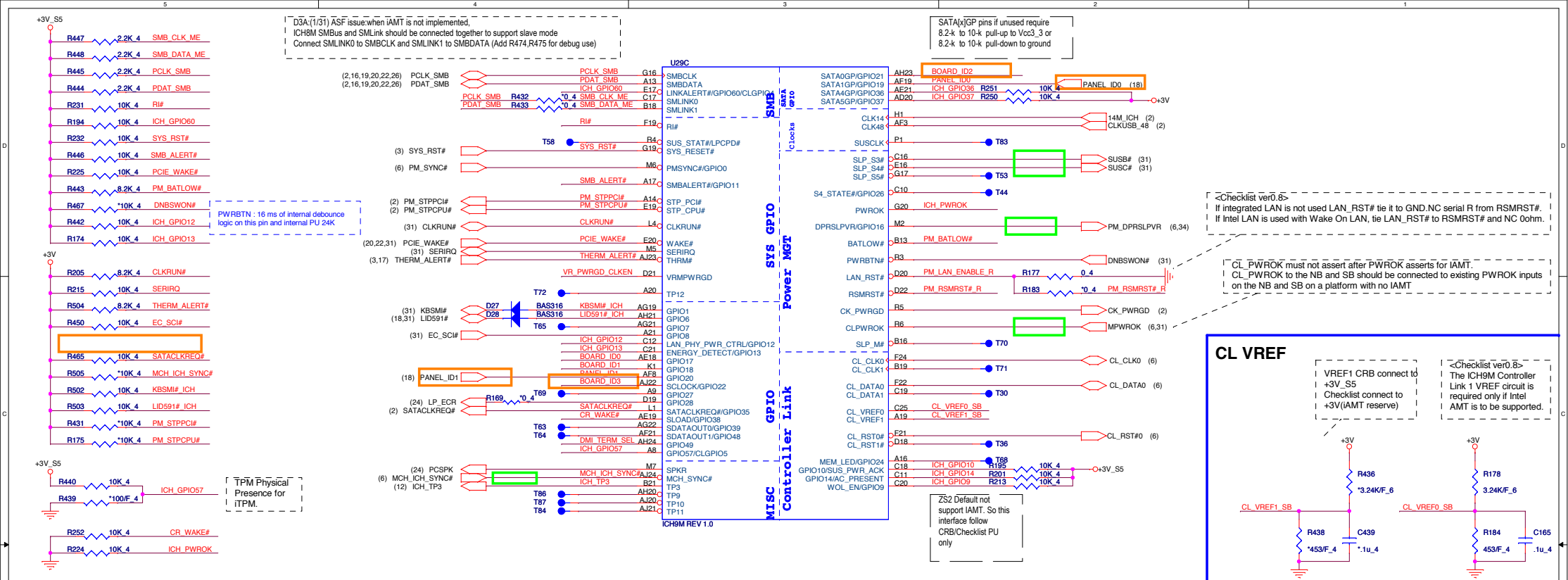


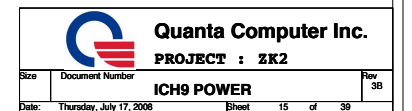
RTC



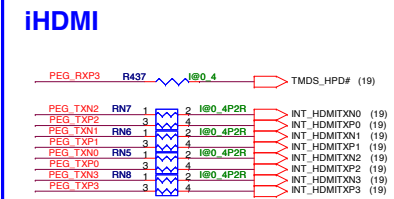
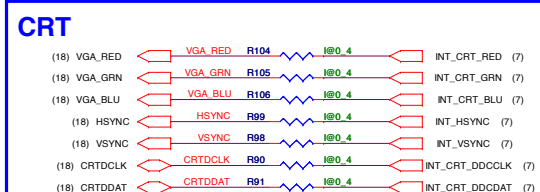
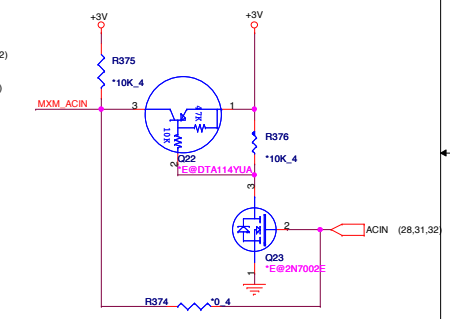
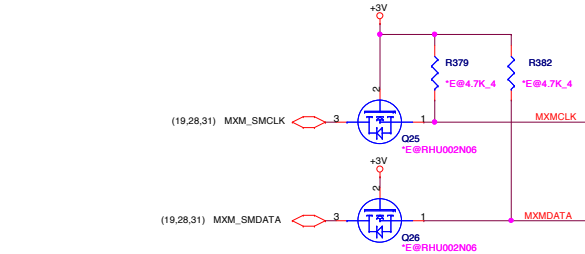
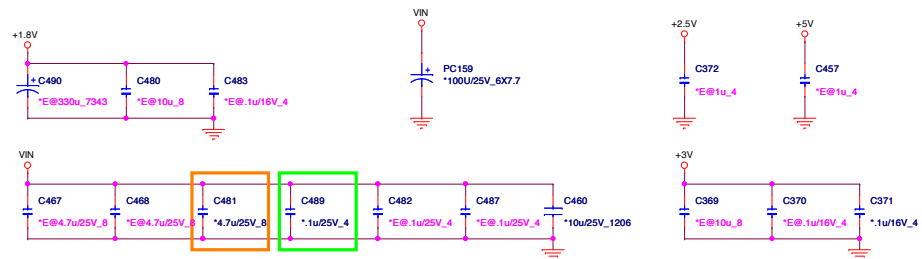
South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description	<p>(14) ICH_TP3</p>
			0	0	RSVD	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	1	Enter XOR Chain	<p>HDA_SDOUT</p>
			1	0	Normal operation(Default)	
			1	1	Secure PCIe Port configuration	





IV@
EV@



IV@
EV@



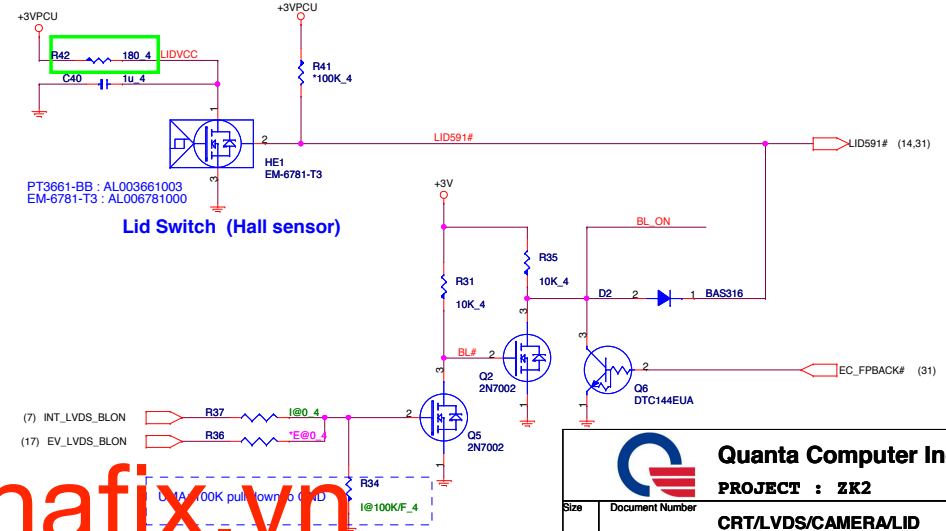
LVDS

P_ID1	P_ID0	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

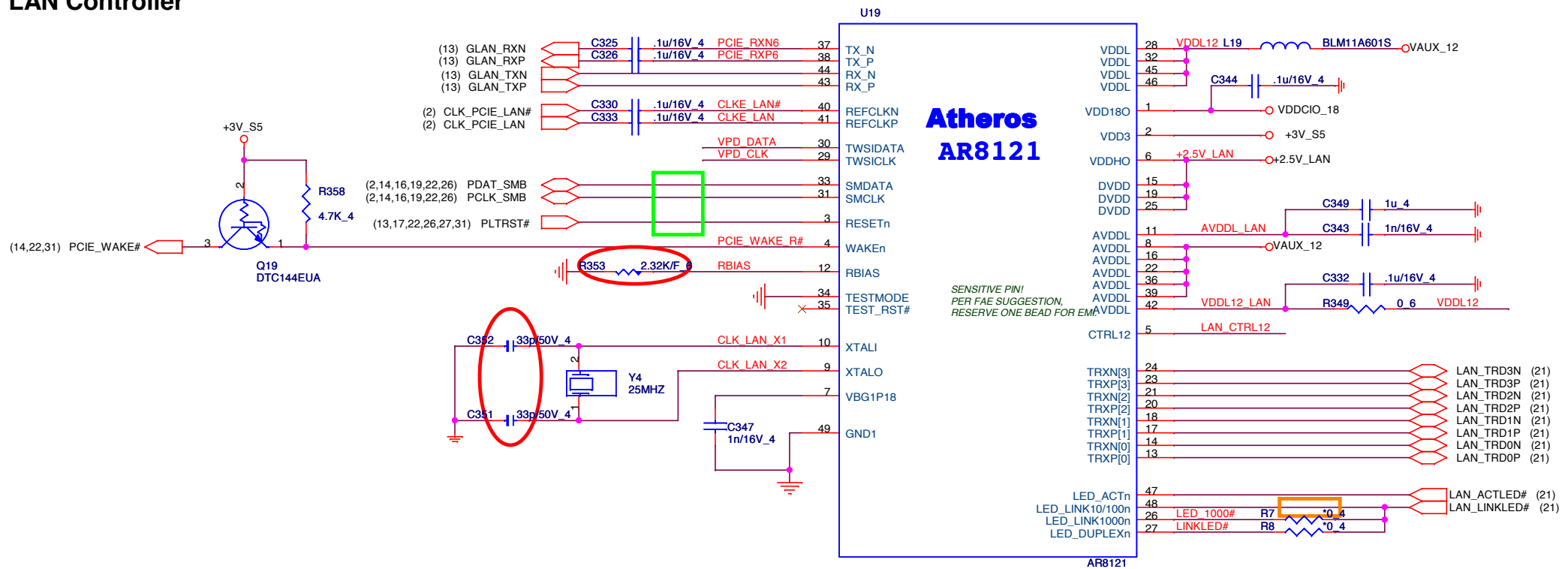
(17) TXCLKOUT+
 (17) TXCLKOUT-
 (17) TXOUT0+
 (17) TXOUT0-
 (17) TXOUT1+
 (17) TXOUT1-
 (14) PANEL_ID0
 (17) TXOUT2+
 (17) TXOUT2-

VIN
 R20 0.8
 R21 0.8
 INVCCP
 +3V
 CCD POWER
 DMIC0_2
 CDD_CLK2
 BL ON
 CN3
 1
 2
 3
 4
 5
 6
 7
 8
 9
 10
 11
 12
 13
 14
 15
 16
 17
 18
 19
 20
 21
 22
 23
 24
 25
 26
 27
 28
 29
 30
 31
 32
 33
 34
 35
 36
 37
 38
 39
 40
 41
 42
 LCD_VCC
 LCD_EDIDATA
 LCD_EDIDCLK
 LCD_VDD
 R362 0.4
 R361 0.4
 R360 0.4
 EV_LVDS_BL_BRIGHT (17) => MX
 L_BKLT_CTRL (7) => UM
 CONTRAST (31) => EC
 USB11+ (13)
 USB11- (13)
 TXCLKOUT+
 TXCLKOUT-
 TXOUT0+
 TXOUT0-
 TXOUT1+
 TXOUT1-
 TXOUT2+
 TXOUT2-
 PANEL_ID1 (14)
 TXOUT0+ (17)
 TXOUT0- (17)
 TXOUT1+ (17)
 TXOUT1- (17)
 TXOUT2+ (17)
 TXOUT2- (17)

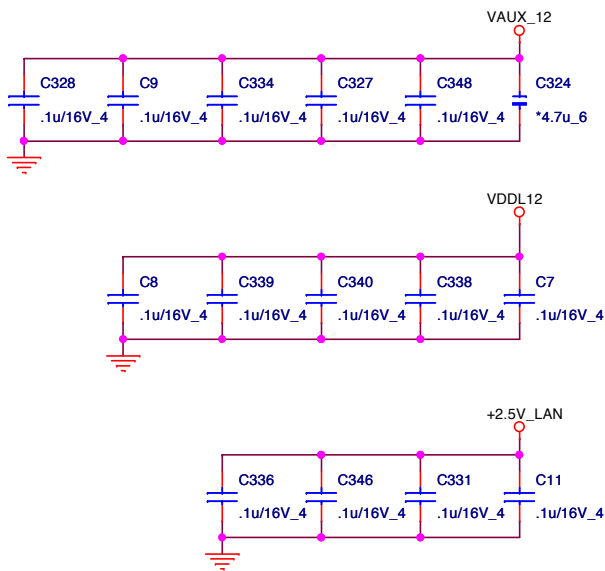
ACES 87241-4001 LVDS



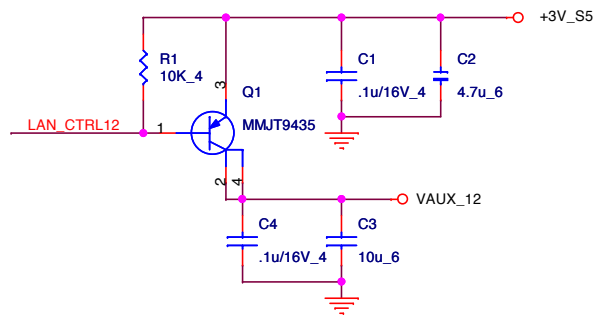
LAN Controller



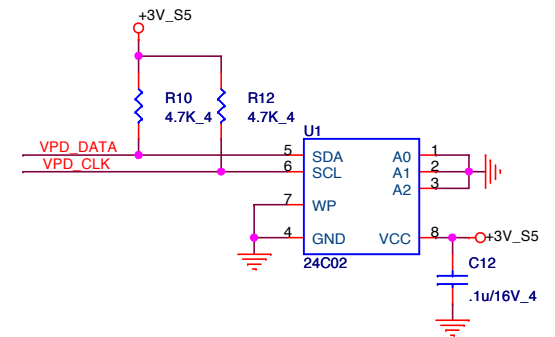
Decoupling CAP



Regulator(1.2V)



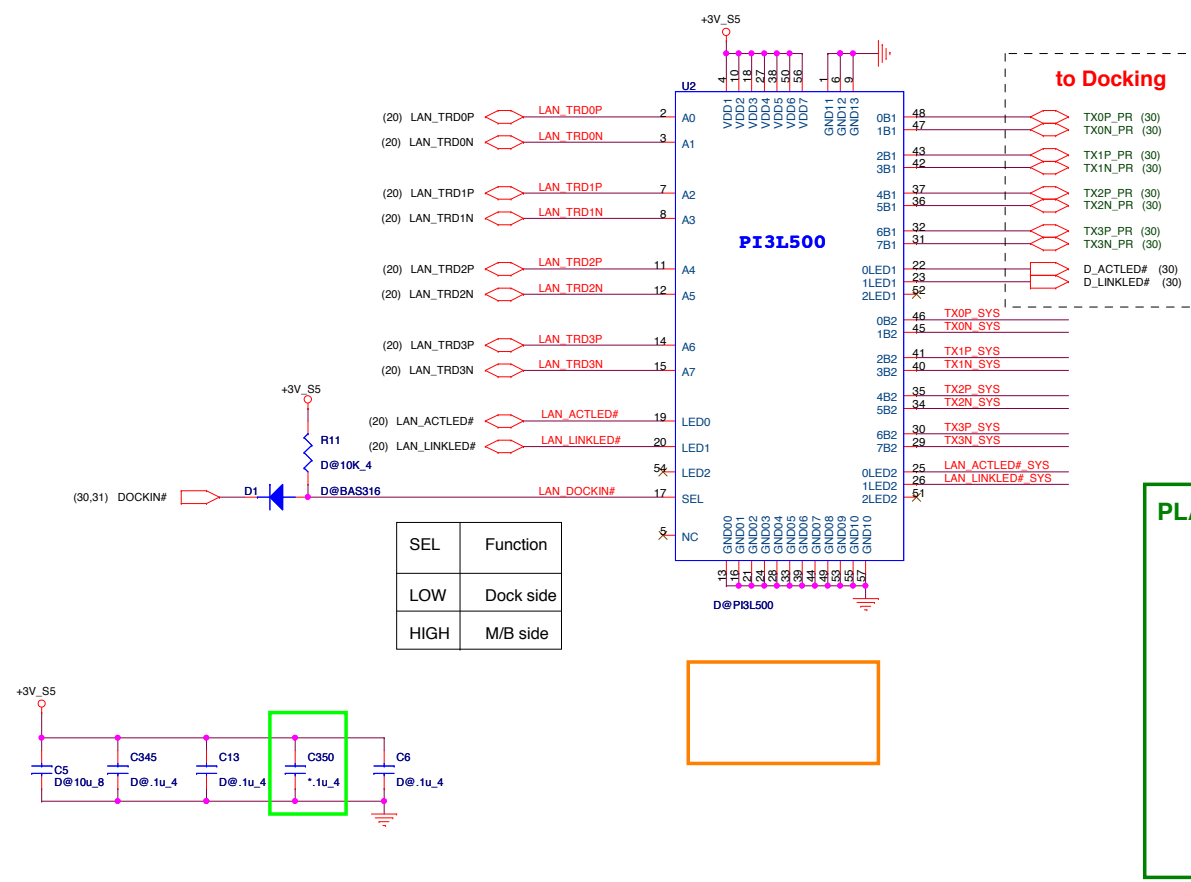
EEPROM



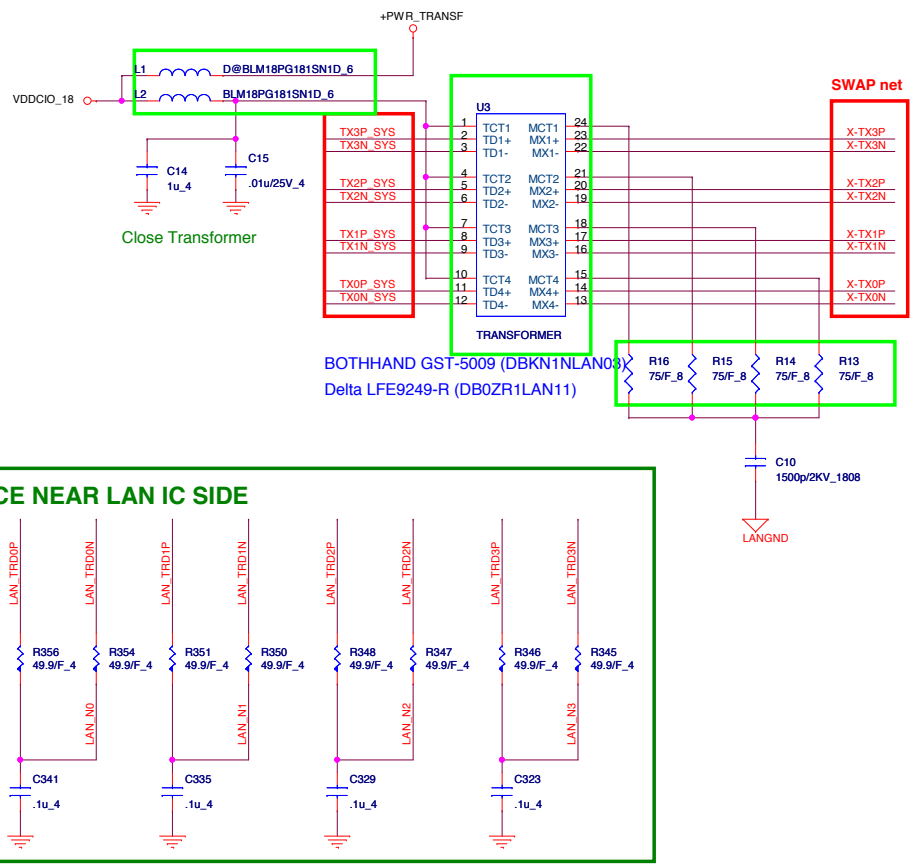
Quanta Computer Inc.

PROJECT : ZK2

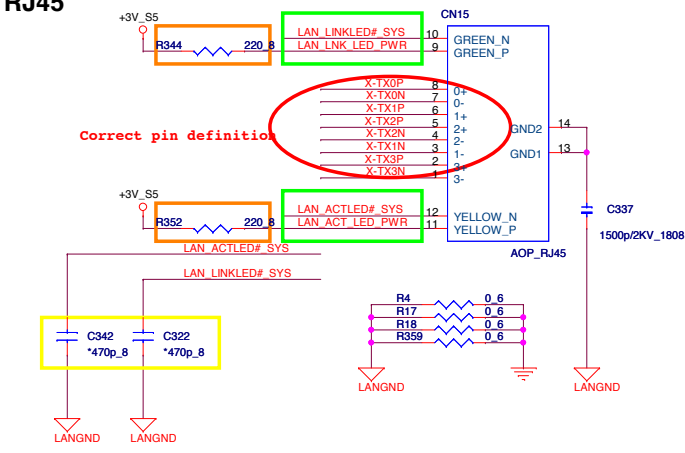
LAN SWITCH



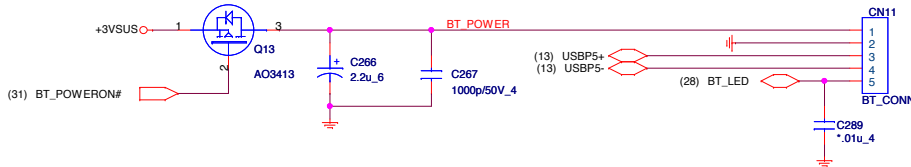
TRANSFORMER



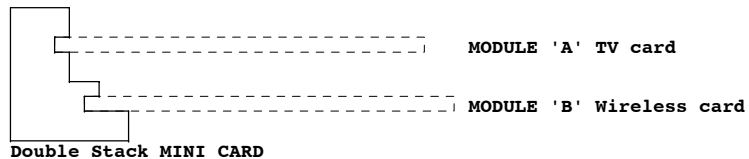
RJ45



BLUETOOTH CONNECTOR



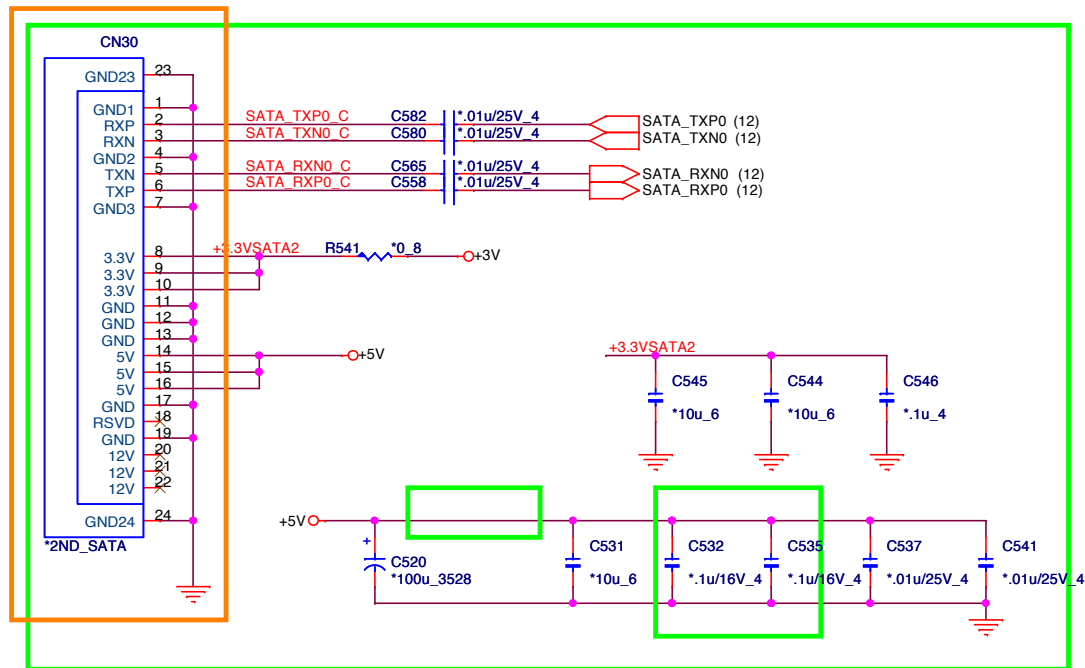
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



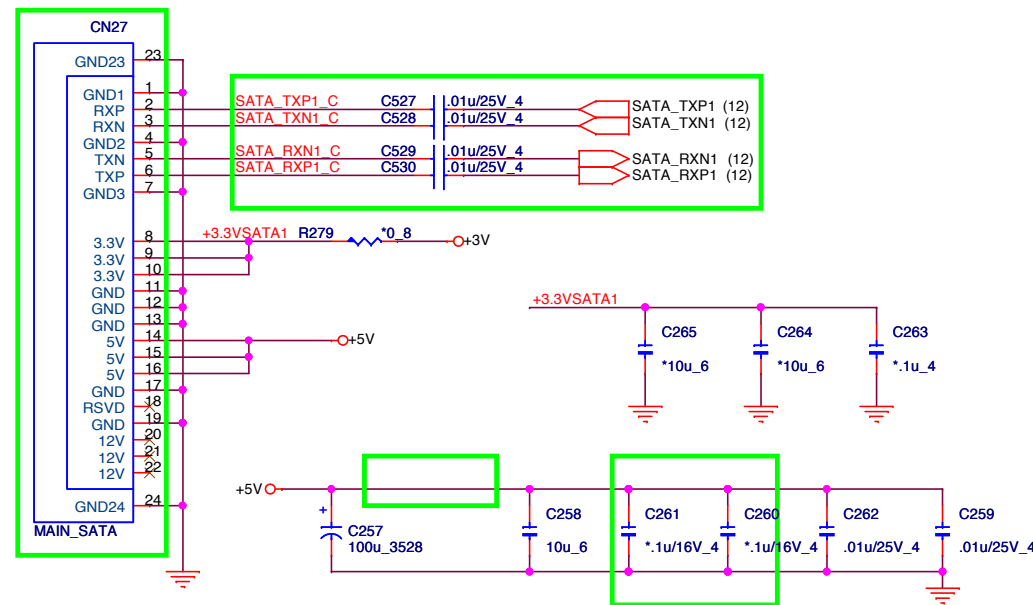
MINI PCI-E card/TV

Size	Document Number	Rev
	MINI PCI-E card/TV	3B
Date:	Wednesday, July 30, 2008	Sheet 22 of 39

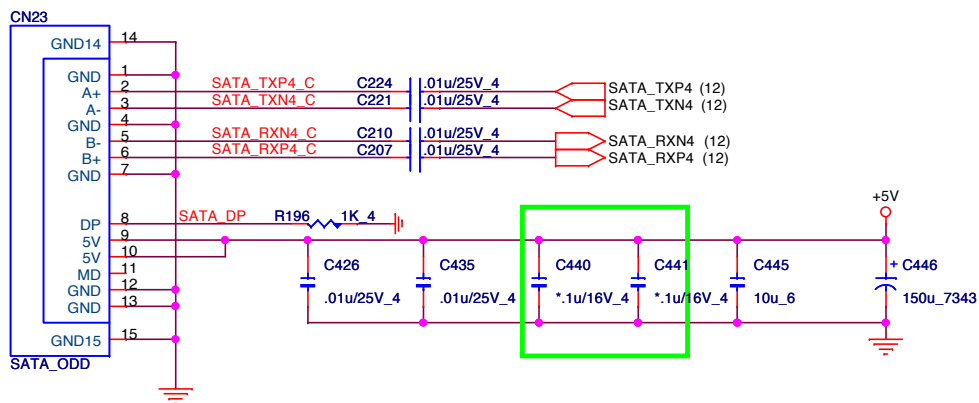
2nd SATA HDD (edge of board)



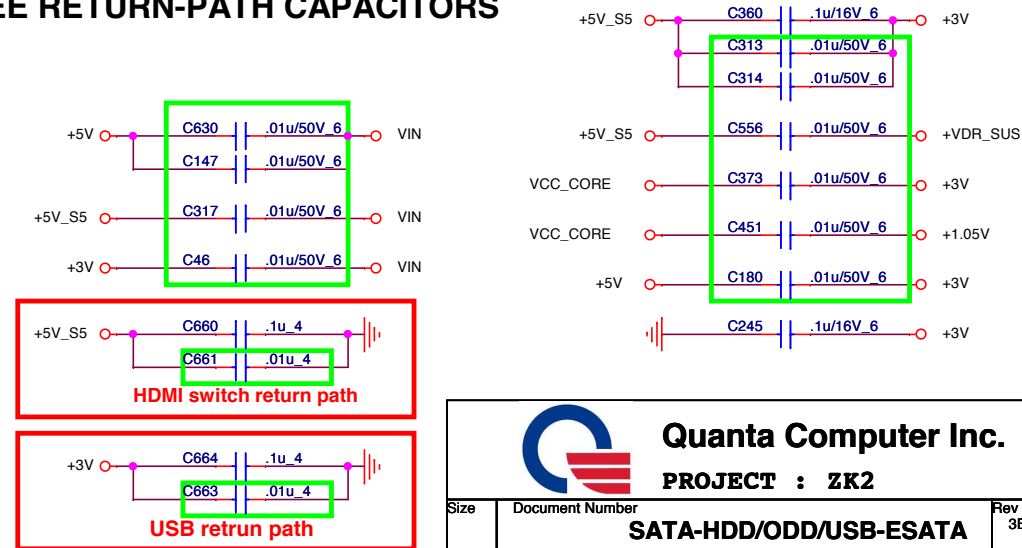
MAIN SATA HDD



ODD (SATA)



EE RETURN-PATH CAPACITORS



Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
Date:	Tuesday, July 15, 2008	Sheet 23 of 39

CODEC(ALC888S)

IV@
EV@

SPK

(25) SURR-L
(25) SURR-R

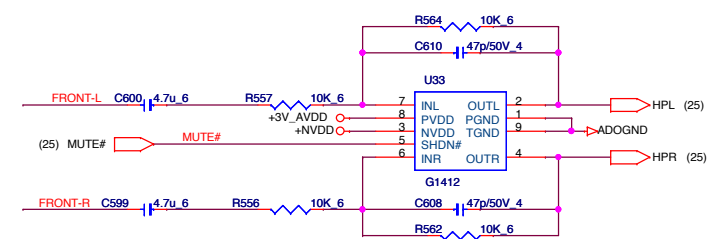
HP

(25) MONO_OUT_L
(25) SPDIF_OUT
(30) SPDIF_DOCK

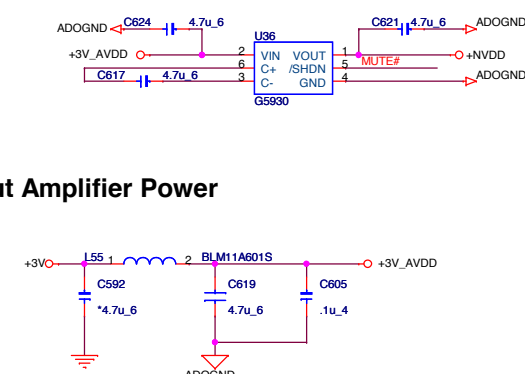
ALC888S-VC

ALC663: US0.65
ALC888S: US0.74

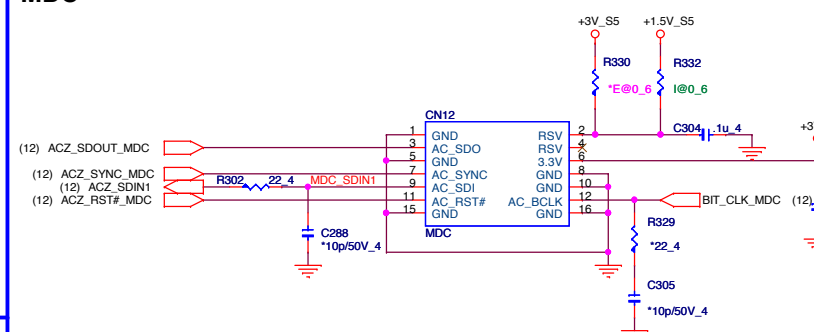
LINE-Out Amplifier



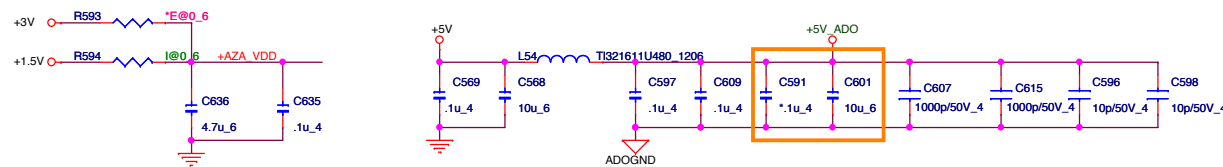
LINE-Out Amplifier Power



MDC



Codec Power



CODEC & MDC

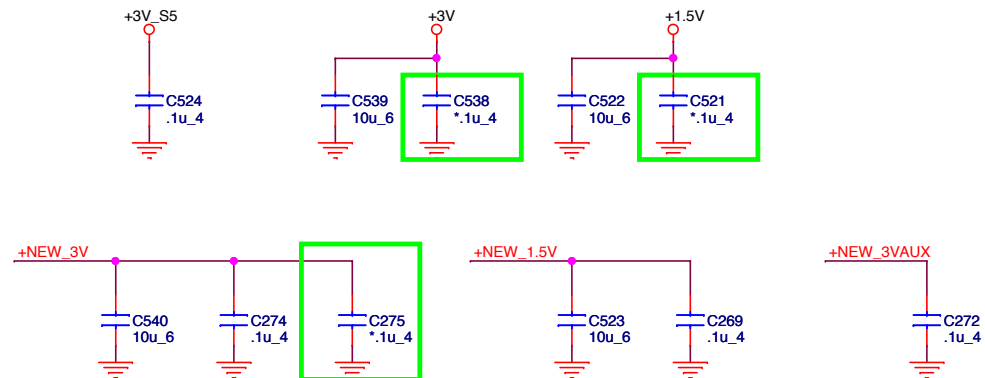
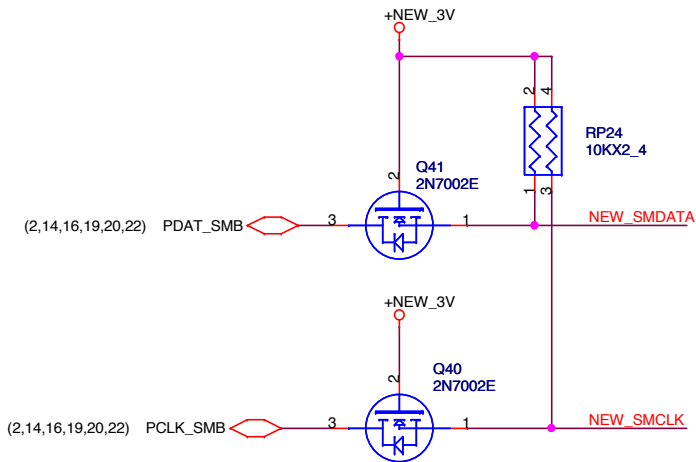
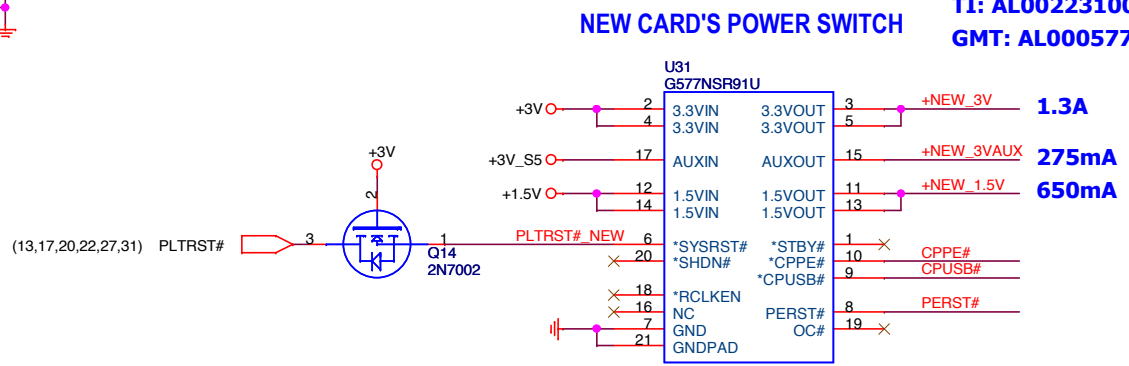
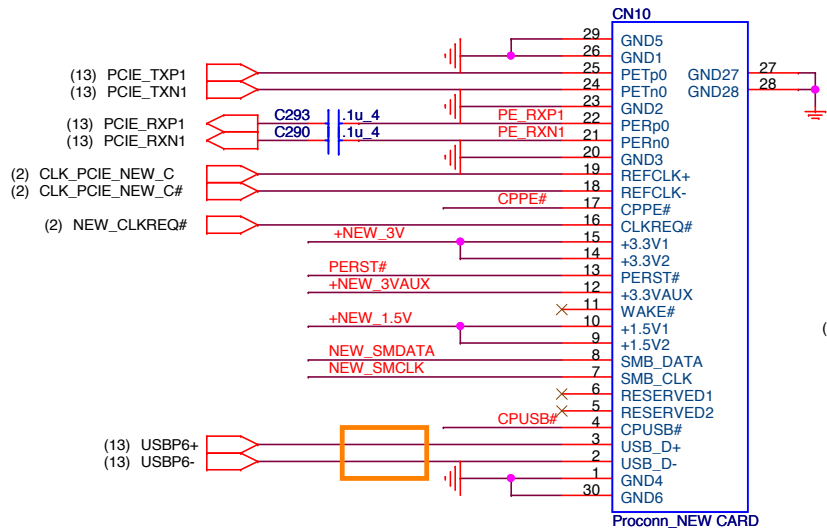
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Size	Document Number	Rev
	REALTEK ALC663&888/MDC	3B
Date:	Tuesday, July 15, 2008	Sheet 24 of 39

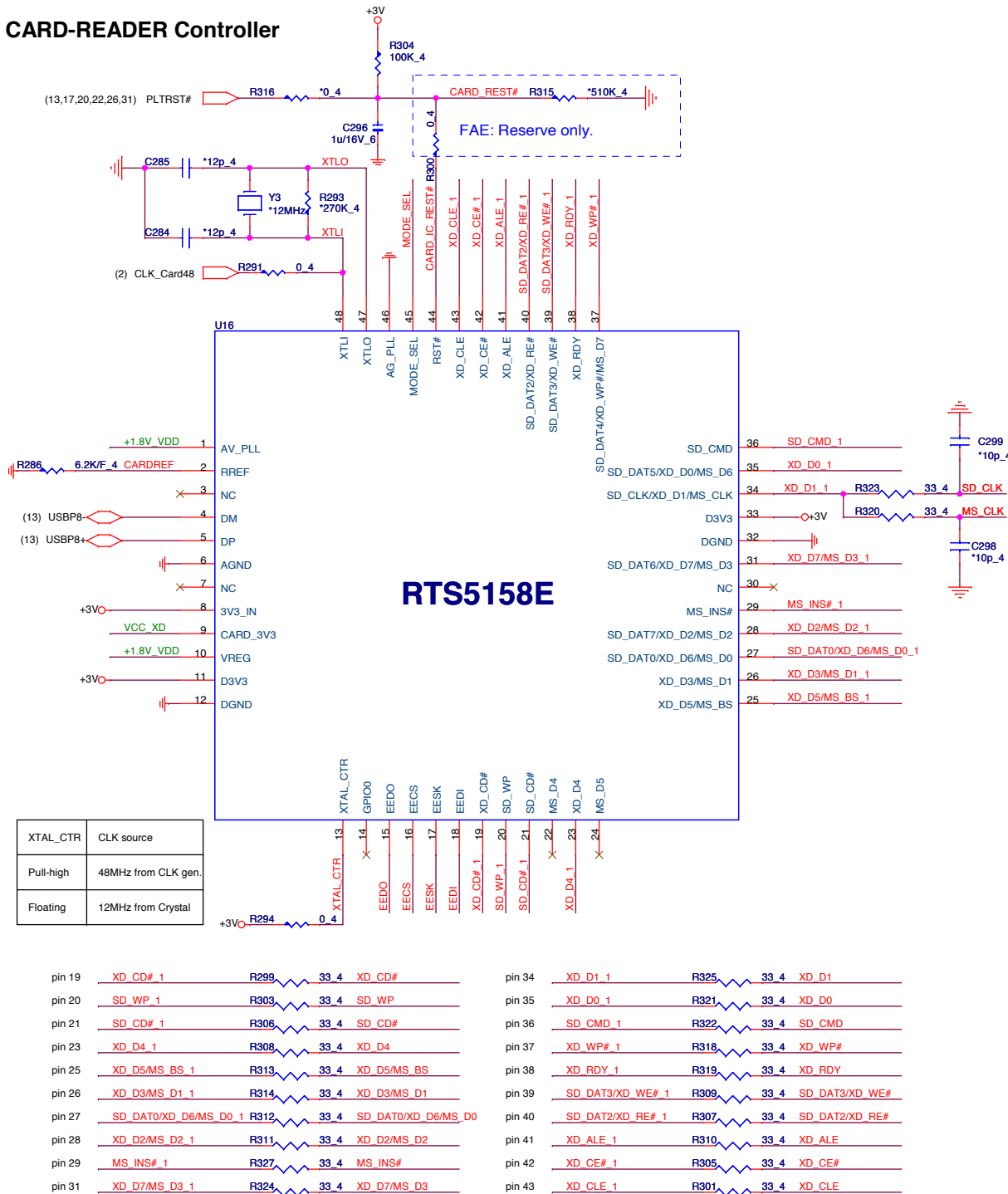
NEW CARD



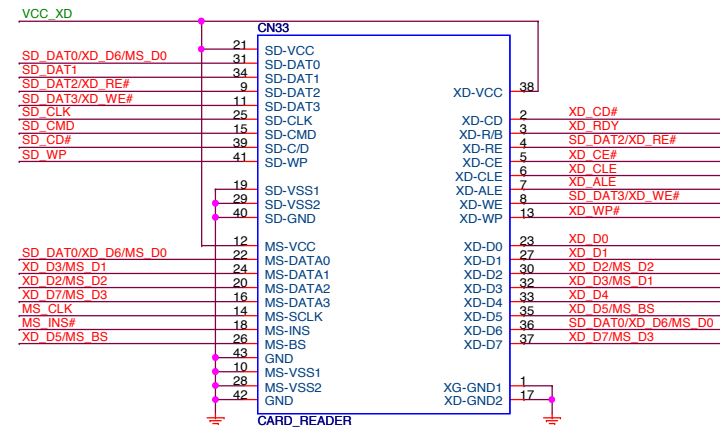
Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	NEW CARD	3B
Date: Saturday, September 13, 2008		Sheet 26 of 39

CARD-READER Controller

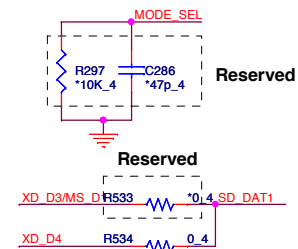


4 IN 1 CARD READER

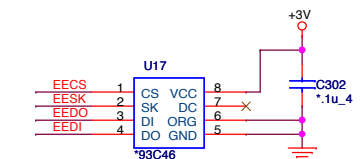


Model Select

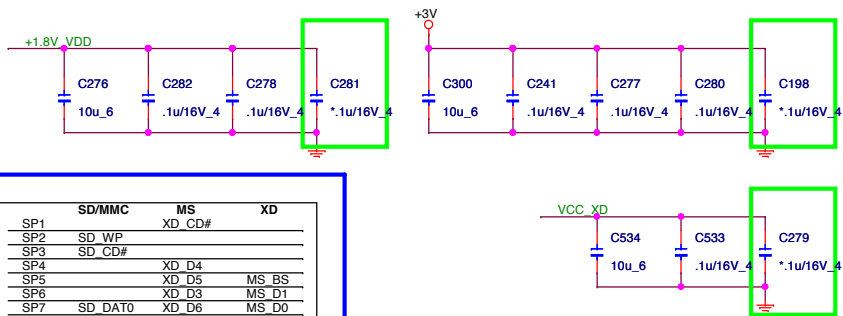
R6256/C860=NC/NC (R6258:ON)=> SD_D1 from pin23
R6256/C860=10K/47pF(R6257:ON)=>SD_D1 from pin26



EEPROM(Reserved)

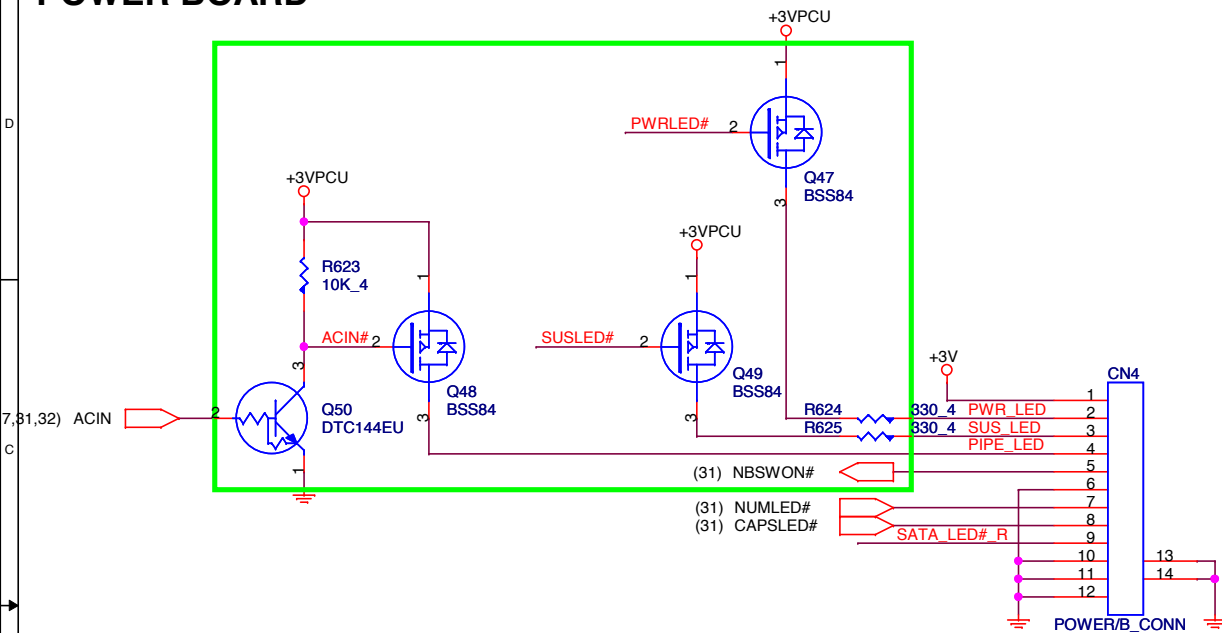


Decoupling CAP

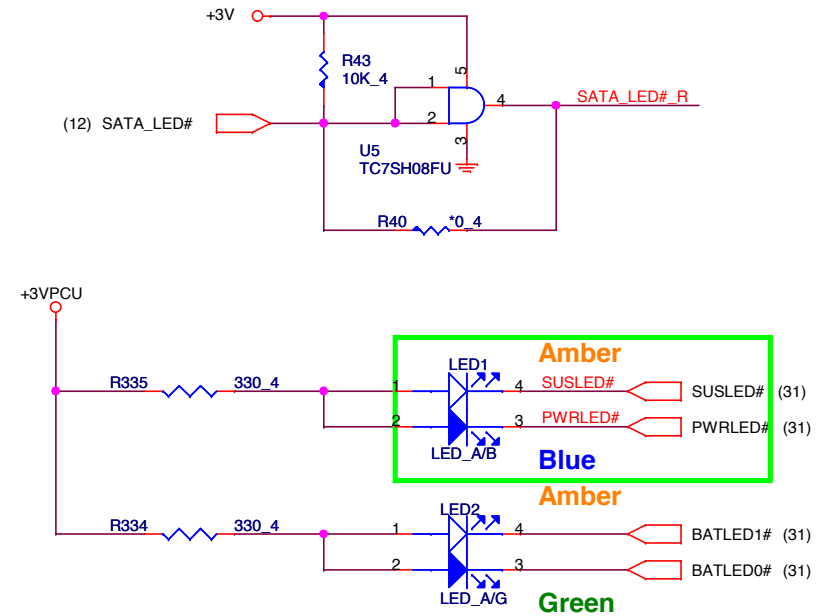


	SD/MMC	MS	XD
SP1		XD CD#	
SP2	SD_WP		
SP3	SD_CD#		
SP4		XD D4	
SP5		XD D5	MS B5
SP6		XD D3	MS D1
SP7	SD DAT0	XD D6	MS D0
SP8	SD DAT7	XD D2	MS D2
SP9			MS INS#
SP10	SD D7	XD D7	MS D3
SP11		XD D1	
SP12	SD DAT5	XD D0	MS D6
SP13	SD DAT4	XD_WP#	MS D7
SP14		XD_RDY	
SP15	SD DAT3	XD_WE#	
SP16	SD DAT2	XD_RE#	
SP17		XD_ALE	
SP18		XD_CE#	
SP19		XD_CLE	
			MS D4
			MS D5

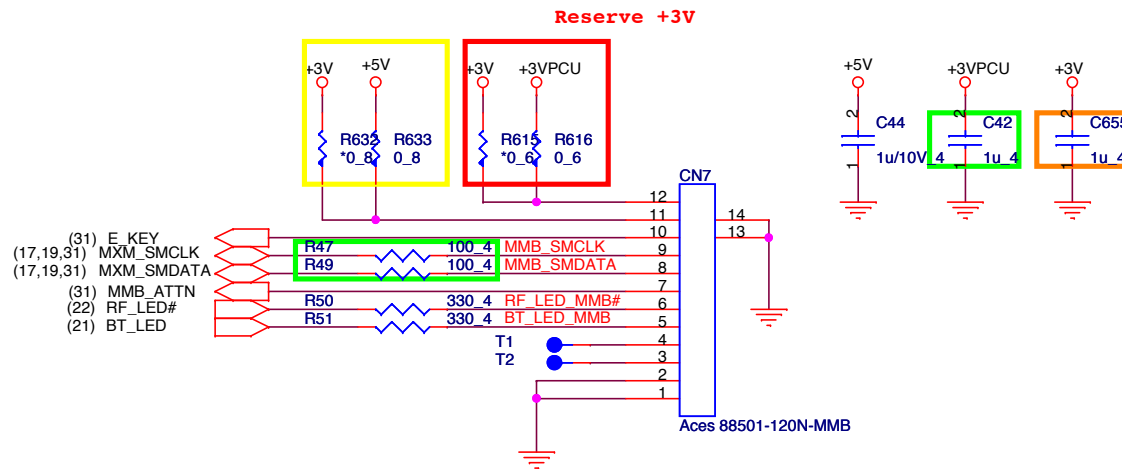
POWER BOARD



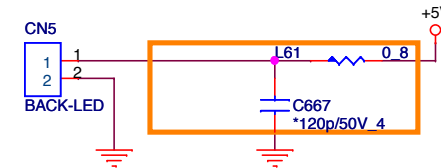
LED




MMB

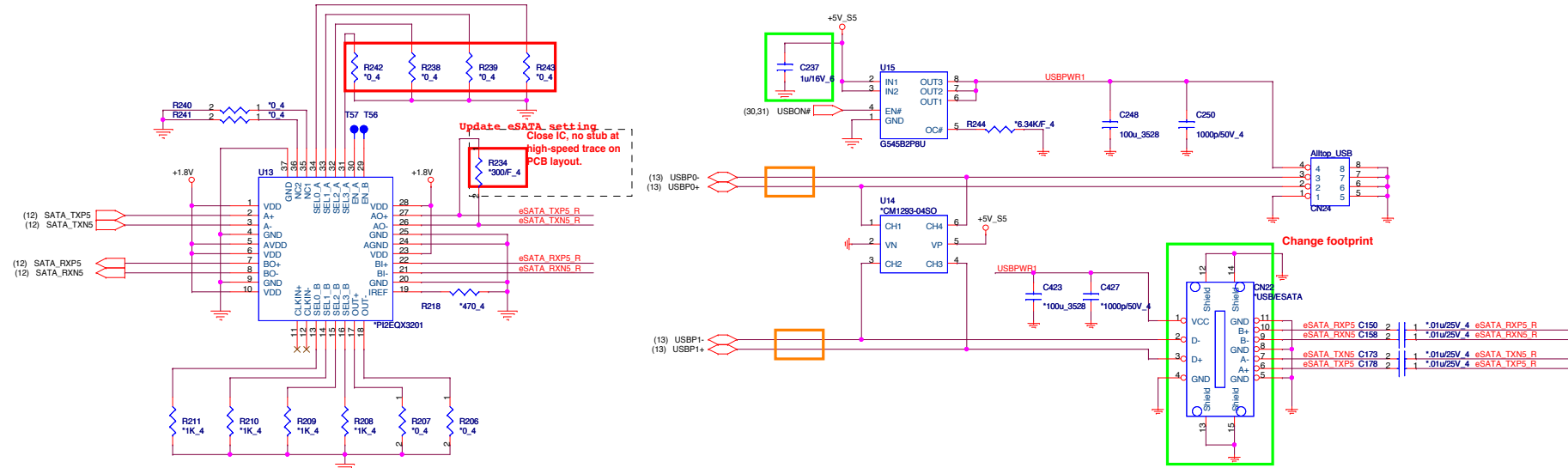


Backlight Logo LED



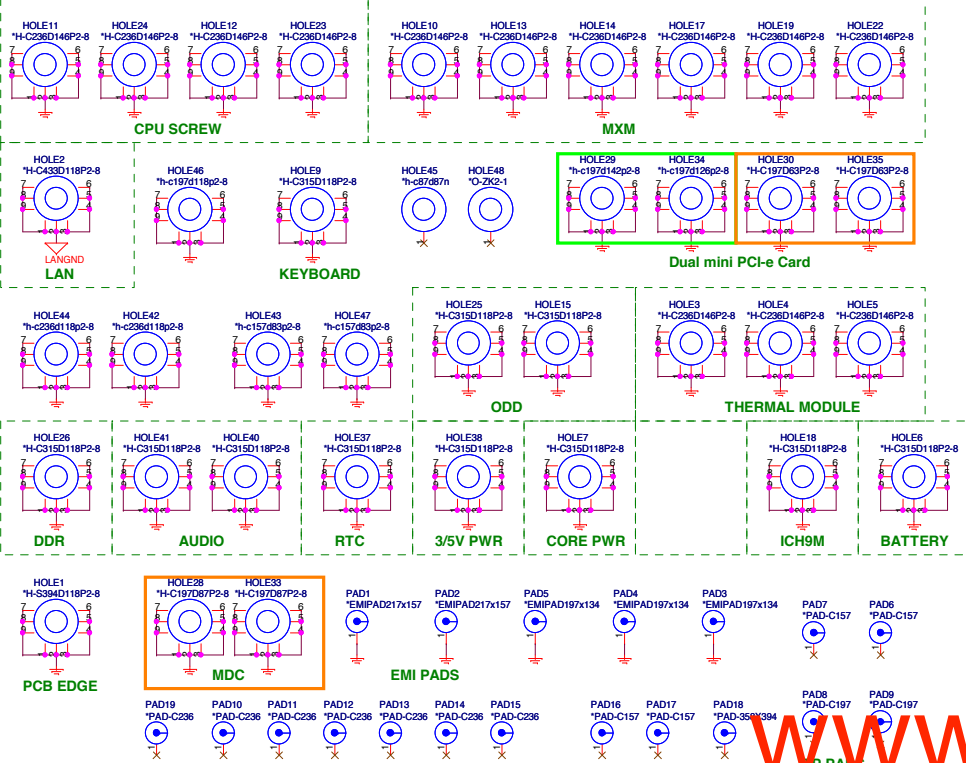
 Quanta Computer Inc. PROJECT : ZK2		Rev 3B
Size	Document Number	Date: Friday, July 25, 2008
Sheet 28 of 39		

USB & ESATA

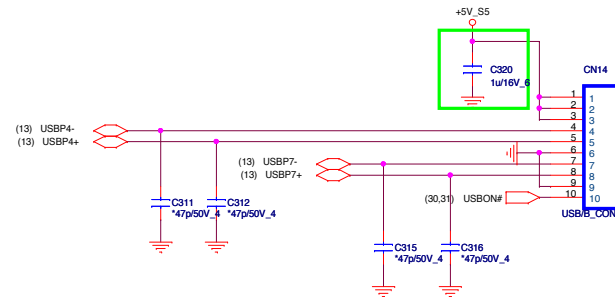


SEL0_X	SEL1_X	E _q	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				

HOLES

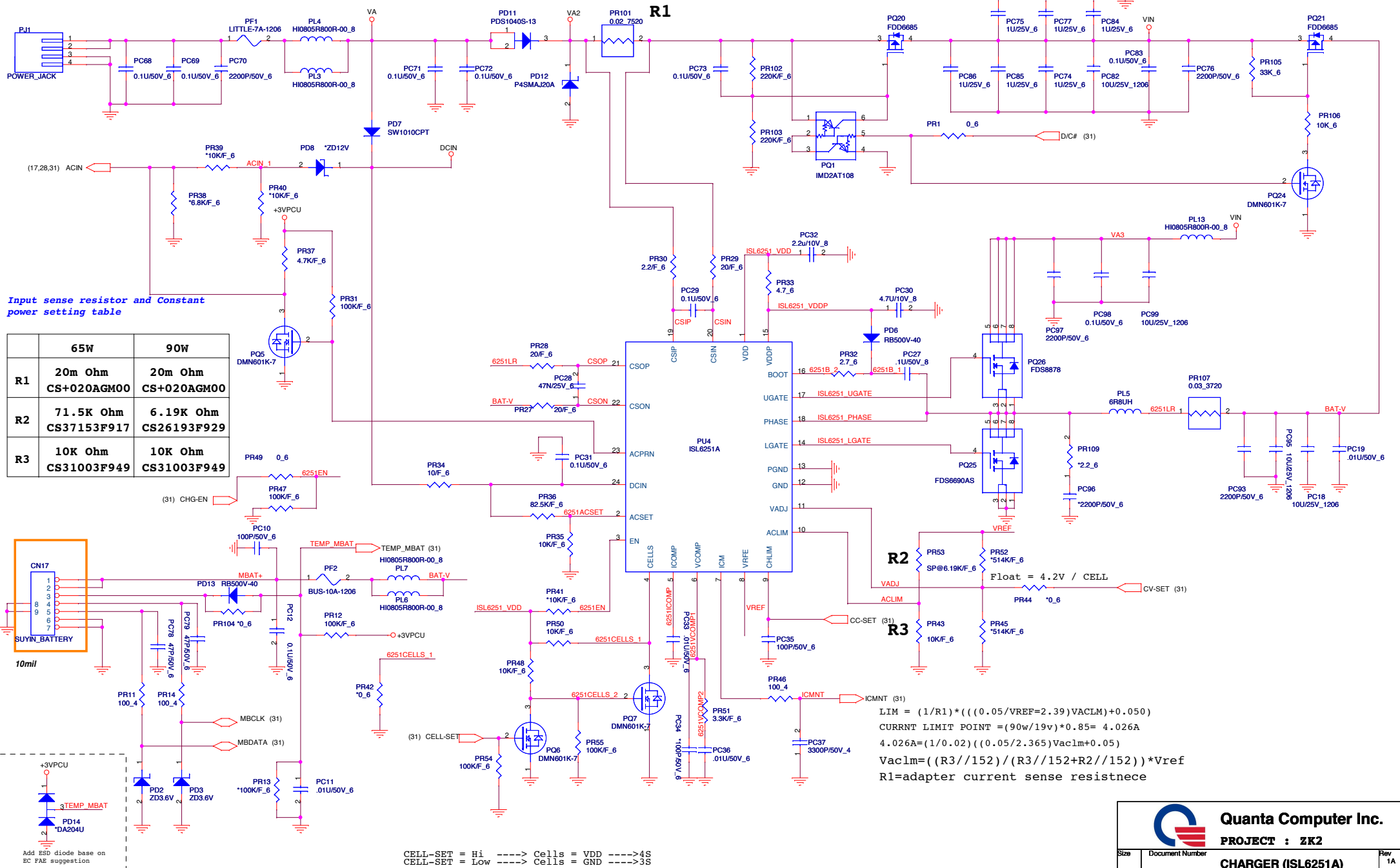


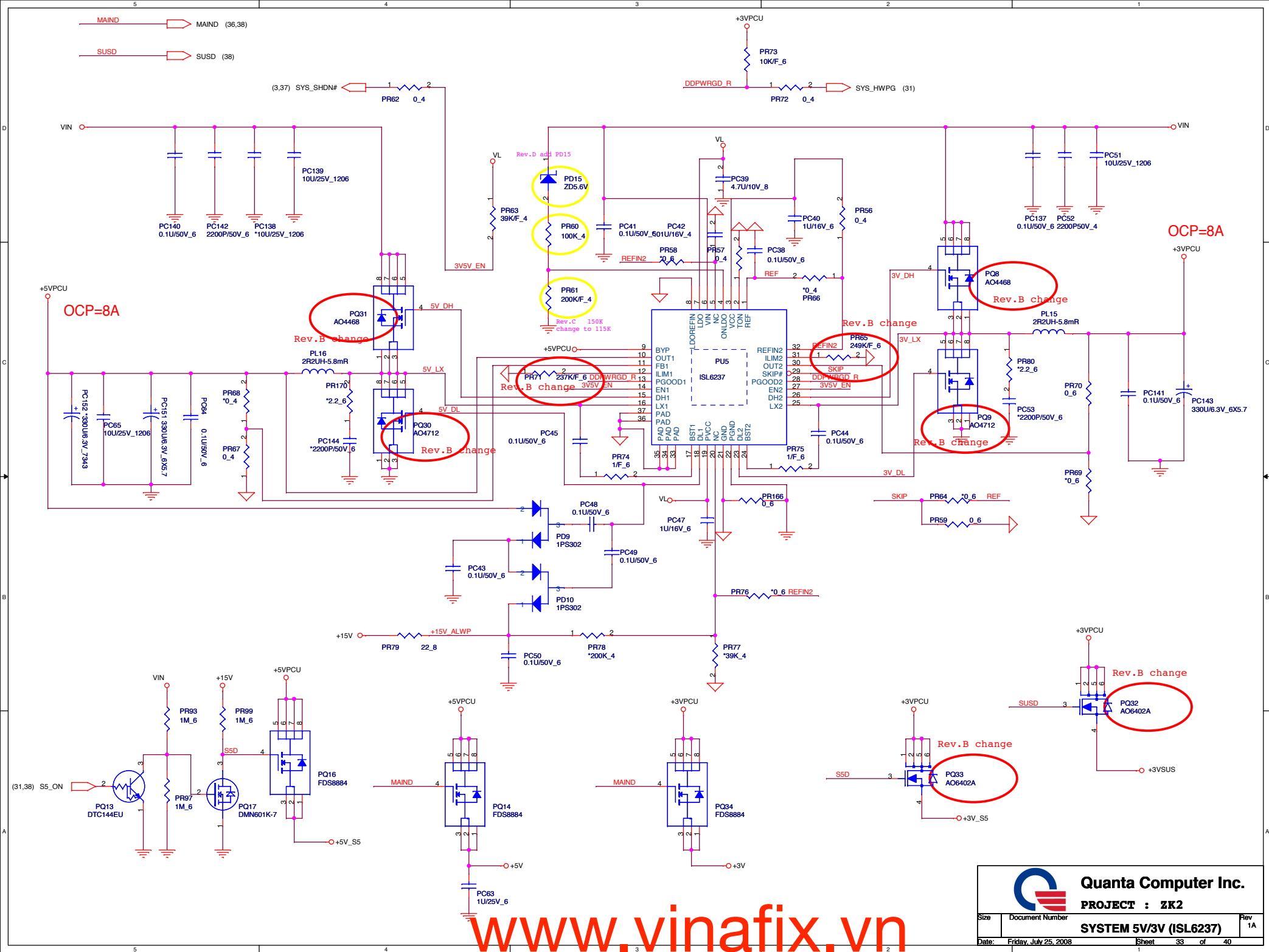
USB/B

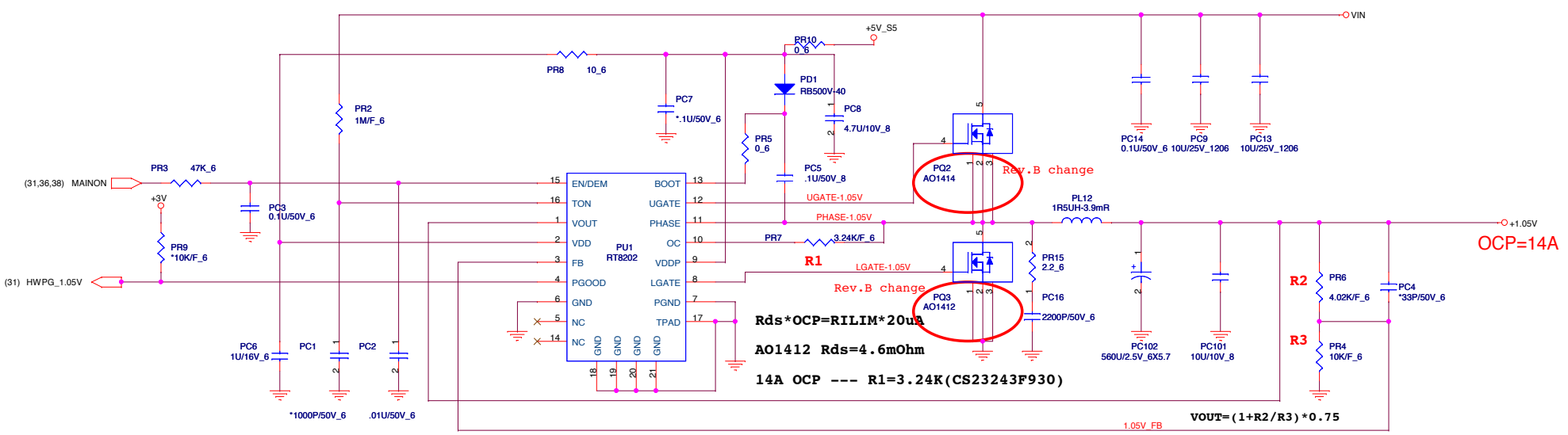


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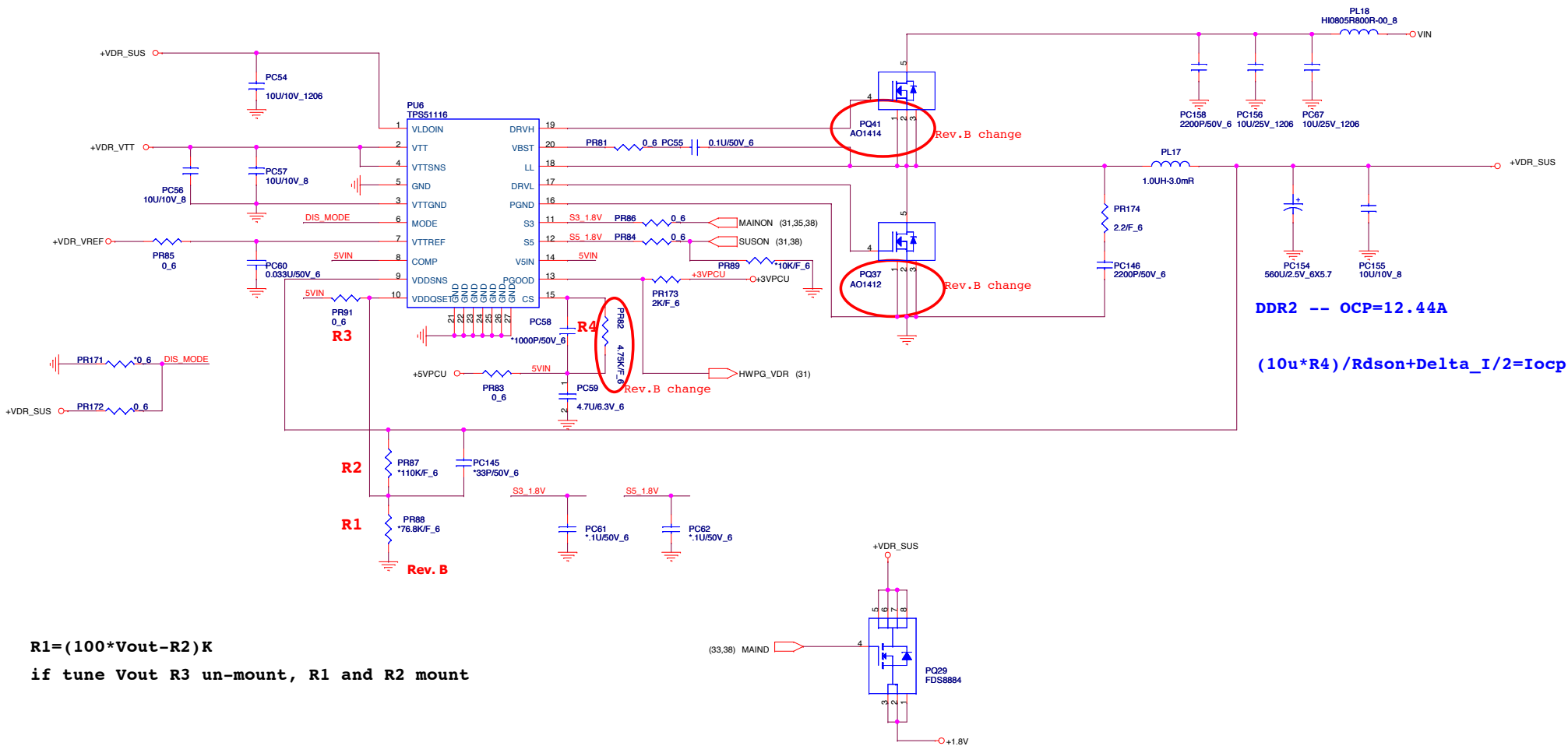




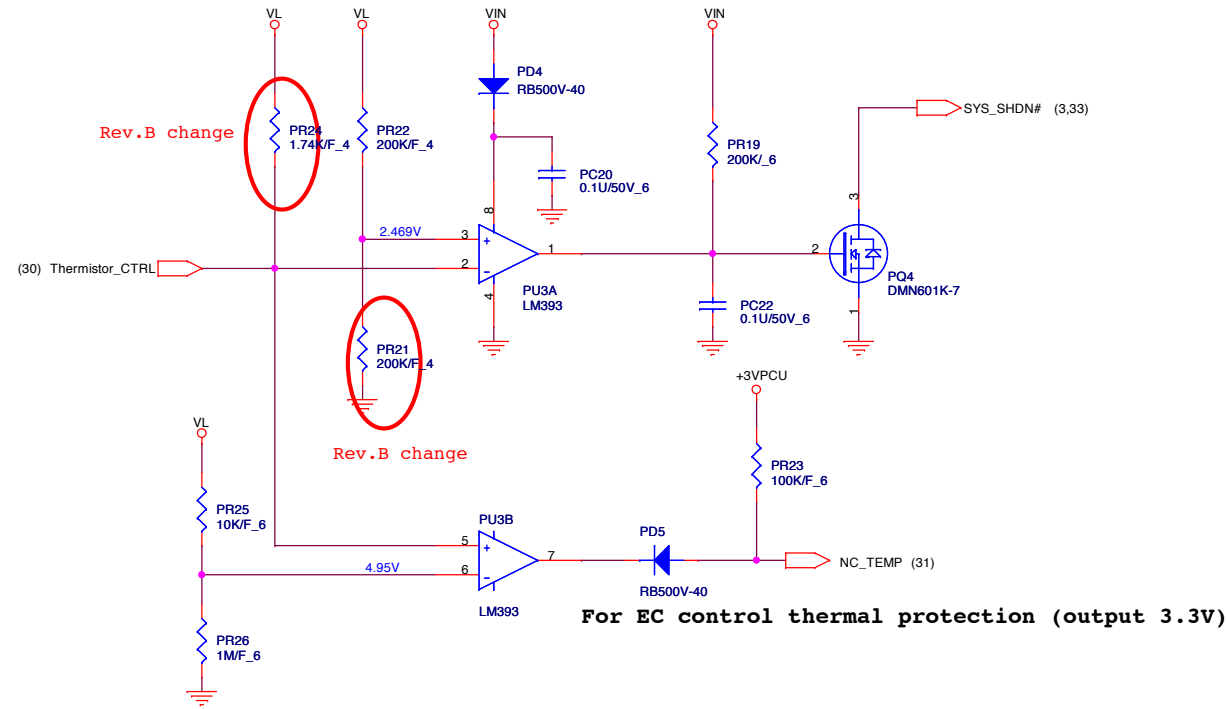



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

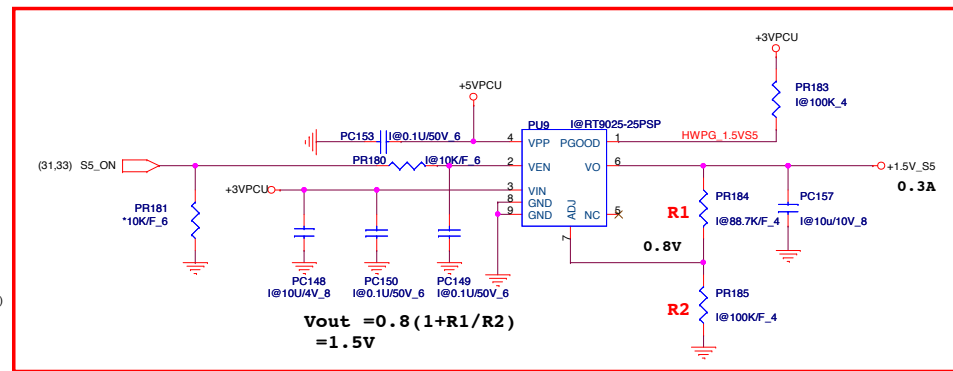
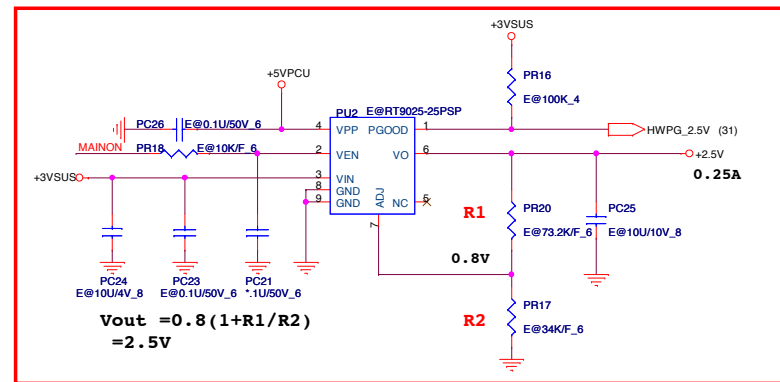
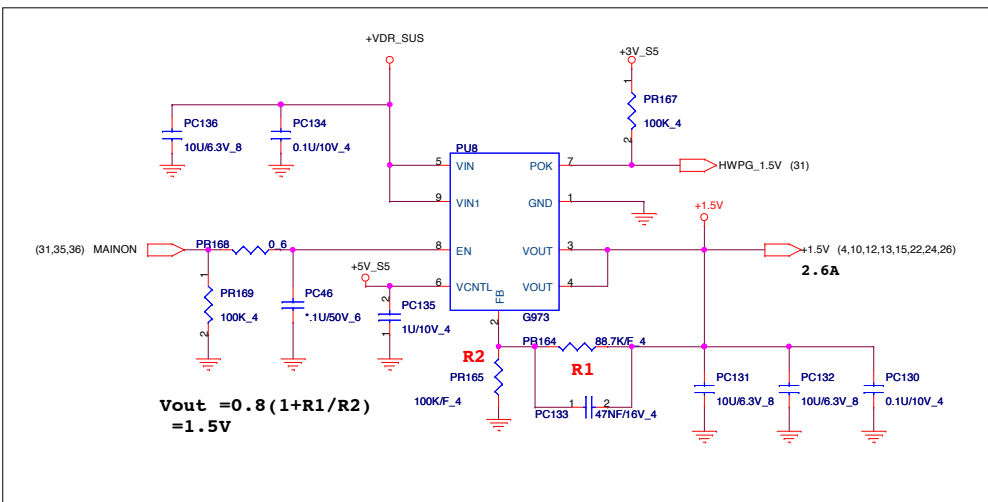
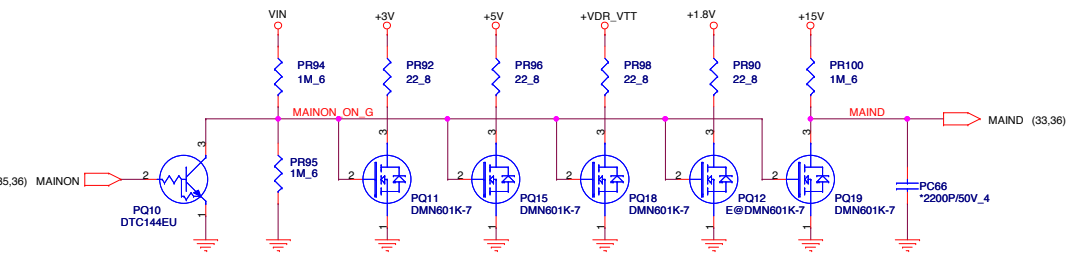
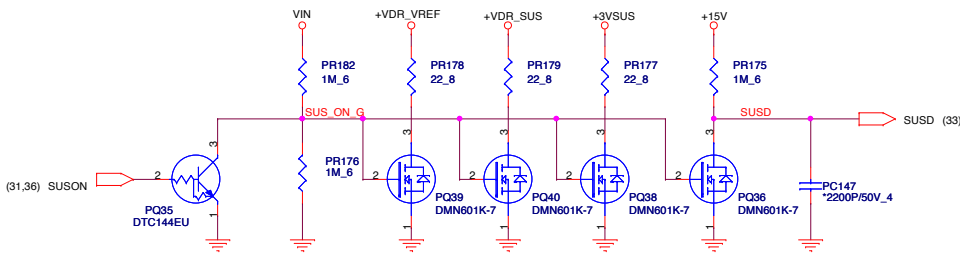
$$Frequency = Vout / (Vin * TON)$$



thermal protection



 Quanta Computer Inc. PROJECT : ZK2		Rev 1A
Size	Document Number	
Thermal protect		
Date: Tuesday, July 15, 2008	Sheet	37 of 40



Model	REV	CHANGE LIST	MODEL	ZK2	
ZK2 MB	1A	FIRST RELEASED: E200803-5424 (PCB: DAOZK2MB6A0)		FROM	To
				X	1A
				X	1A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
2A		Page10 : Correct LVDS power of NorthBridge to +VDS SUS Page11 : Change 32.768KHz (Y2) to normal type(R13.5) Page12 : Change EMI filter connector type (C814) to DFWD02MR311 Page17 : Swap SATA port between port-1 (DD0) and port-4 (2ND HDD) Page18 : Change LCD power input capacitor (C27) to 2.2uf Page19 : Change all HDMI switch solution to Parade (P80122), and connector type to DIP type Page20 : Correct LAN R185 (R235) to 2.2Kohm to improve performance and signal quality Page21 : Correct X'ral capacitor (C351/C352) to 33pf for 45MHz Page22 : Change LAN R185 for EMI and correct R185 connector pin definition for wrong connect Page23 : Change L42 to 0ohm resistor Page24 : Add 200.1uf electrolytic capacitor (C660/C661) for HDMI switch Page25 : Change L4C solution for SPDIF and DMIC EMI issue Page26 : Correct GPIOIP (C825) pin definition Page28 : Change power/B power source to +3V only Page29 : Reserve +3V power source for MM function Page29 : Modify eSATA controller (U13) swing/EQ/de-emphasis setting for signal quality, and correct eSATA connector type Page29 : Move 0oh power switch to USB/B Page29 : Change finger-printer power source to +3VSUS		1A	2A
		Power change items		1A	2A
		Page32 : [PR53] 6.19Kohm(C826193P929) for MM(90W ADP) Page32 : 71.5Kohm(C837153P917) for UMA(60W ADP)		1A	2A
		Page33 : 1. Change PQ31/PQ8 from FDS8878(BAM88780020) to A04468(BAM44680003) 2. Change PQ30/PQ9 from FDS6690AR(BAM66900022) to A04712 (BAM47120000) 3. Change PQ32/PQ33 from FDC53 (BAM65300023) to A04602A (BAM64020000) 4. Change PR61 from 150K/F_4(C841502FB18) to 150K/F_4(C841502JB10) 5. Change PR71 from 178K/F_6 (C841783FP918) to 237K/F_6 (C842373FP911) 6. Change PR65 from 196K/F_6 (C841963FP916) to 249K/F_6 (C842493FP914)		1A	2A
		Page34 : 1. Change PQ27/PQ22 from TPCAR021-H (BAM80210000) to A01414 (BAM14100001) 2. Change PQ28/PQ23 from TPCAR019-H (BAM80190000) to A01412 (BAM14120000) 3. Change PC111 from 0.022u/50V_6 (CH3226K1901) to 0.033u/50V_6 (CH3336J1900)		1A	2A
		Page35 : 1. Change PQ2 from TPCAR021-H (BAM80210000) to A01414 (BAM14100001) 2. Change PQ3 from TPCAR019-H (BAM80190000) to A01412 (BAM14120000)		1A	2A
		Page36 : 1. Change PQ41 fromTPCAR023-H (BAM80230000) to A01414 (BAM14100001) 2. Change PQ37 from TPCAR019-H (BAM80190000) to A01412 (BAM14120000) 3. Change PR82 from 5.62K/F_4 (C825623FP914) to 4.75K/F_6 (C824753FP919)		1A	2A
		Page37 : 1. Change PR21 from 196K/F_4 (C841962FB01) to 200K/F_4_4(C842002FB12) 2. Change PR24 from 1.43K/F_4 (C821432FB00) to 1.74K/F_4 (C821742FB00)		1A	2A
				2A	3A
				2A	3A
3A		Page2 : no mount 0.1uf (C475/C492/C471) Page4 : no mount 0.1uf (C153) Page11 : remove 0 ohm (R160/R330/R402/R159), and connect them directly Page12 : remove 0 ohm (R458/R249/R487), and connect them directly Page13 : Swap Main HDD to port-0, and 2nd HDD to port-4 Page13 : remove 0 ohm (R198), and connect them directly Page14 : Swap USB port2 to external USB, and port-7 to Cardreader Page14 : remove 0 ohm (R186/R185/R466/R235/R506), and connect them directly. Page15 : no mount 0.1uf (C170/C448) Page16 : no mount 0.1uf (C230/C252) Page16 : reserve 0 ohm (R629) from MM to EC (EC_THERM#) Page17 : no mount 0.1uf (C489) Page18 : no mount Q1/Q04 and bypass from 0ohm (R378/R381), pull-up 2K ohm to +3V for MM sku Page18 : Change L6/7/8 to BLM188A470RN1D Page18 : Change U4 to AL004280001 (AAT4280-4) part Page18 : Remove 0 ohm (R23), and connect directly Page18 : Change CN3 to DFHW40MR000 for SMT request Page19 : Change R42 from 330 ohm to 180 ohm (C811802JB15) Page19 : Use 100 ohm (R619/R620/R621/R622) and 1pf (C656/C657/C658/C659) for HDMI EMI request Page19 : Reserve C662/Q43/Q44/R119/R126, and bypass 0ohm (R627/R628) Page20 : remove 0ohm (R5/R9/R357) and connect directly Page21 : Change L1/L2 (BLM180181RN1D) to increase current rating Page21 : Change transformer to GST-5009 Page21 : Change R13-R16 from 75ohm Q402 to 0805 size Page22 : no mount 0.1uf (C390) Page22 : Swap LAN LED color connect (green: linking/orange:active) Page22 : Remove R296/R292/R328/L42/R298 and connect directly Page23 : no mount 0.1uf (C247/C270/C268) Page23 : Change main (CN27) and 2nd (CN30) HDD footprint for M/E request Page23 : no mount 0.1uf (C532/C535/C260/C261/C480/C441) Page24 : Change 0.1uf to 0.01uf (C630/C14/C313/C46/C661/C663/C313/C314/C556/C373/C451/C180) Page24 : remove 0ohm (R574) and connect directly Page25 : no mount 0.1uf (C281/C198/C275) Page25 : no mount 0.1uf (C281/C198/C275) Page26 : Add 10uf LED-ON function (Q49/G50) Page28 : Add PWLED/SUSLED function on Power/B (Q47/Q49/R624/R625) Page28 : Change R47/R49 from 0ohm to 100ohm for synaptic MM Page29 : Change R59/R58 from 0ohm to 100ohm for +3V/Amber Page29 : Change R59/R58 from 0ohm to 100ohm for +3V/Amber Page29 : Change e-SATA connector (CN22) Page29 : Add 10uf (C666) for TV Page30 : Update incorrect hole29/hoec14 footprint Page30 : no mount 33pf (C33/C34) Page31 : Remove L24/L25/L26 and connect directly Page31 : no mount 0.1uf (C60/C65/C400) Page31 : Change SW1 to short-pad (G3) for easy power-on Page31 : Change U38 to everlight part (IRM-V538-TRI)		2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
				2A	3A
3B		Page8 : update SB p/n to AJ8L8940T04 (GH45), AJ8L8970T06 (PH45) Page9 : remove 0 ohm (R167), and connect them directly Page10 : Add 10uf capacitor (C665/C193) for CRT flicker issue Page12 : remove 0 ohm (R247), and connect them directly Page14 : update SB p/n to AJ8L8940T03 Page14 : Add panel_ID0 (GPIO19)/1 (GPIO20) on SB, and pull-up 10Kohm (R629/R630) to +3V near LCD connector (CN3) Page14 : Change Board_ID2 to GPIO21, and Board_ID3 to GPIO22 Page15 : Remove R516 Page17 : no mount 4.7uf capacitor (C481) Page17 : remove 0 ohm (R176/R472), and connect directly Page18 : delete no-dock CRT resistor, no mount 0.1uf (C49) Page18 : remove 0 ohm (R617/618), and connect directly for USB Page19 : Add panel_ID0 (CN3.35) and panel_ID1 (CN3.30) Page19 : reserve 100 ohm (R634/R635/R636/R637) Page20 : Remove 0 ohm (R59/R64) and connect directly Page20 : remove 0ohm (R355) and connect directly Page21 : delete no-dock LAN resistor Page22 : Change R344/R352 to 220 0805 size for RMA request Page22 : Remove RP11/RP10/R545 and connect directly Page22 : Reserve Q51 and bypass 0ohm (R631) Page23 : Add 10uf (C666) for TV Page23 : Update new footprint (CN30) library issue Page24 : no mount 0.1uf (C591) and add 10uf Page24 : Change C601 from 4.7uf to 10uf Page25 : Change MUTE function circuit to AMD gate (U42), and reserve bypass 0ohm (R638) Page25 : remove 0 ohm bridge resistor (R540/R546/R552/R553/R555) to reduce noise Page25 : Change R570 from 20Kohm to 12.4Kohm for subwoofer gain issue Page25 : remove 0ohm (R575) and connect directly Page25 : Change C623 from ADOOND to GND Page25 : Change C516/C525 from 47nf to 470pf Page26 : Remove 0ohm (R77/R277) and connect directly Page26 : Use +3V power (R632) for MM and Reserve +5V (R633) Page26 : Add 1uf (C655) for +3V power Page29 : Remove R45 and connect directly, reserve L61/C667 for EMI request Page29 : Remove 0ohm (R609/R610/R611/R612) and connect directly Page29 : Increase 0.1mm width for Hole28/33/30/35 Page30 : Change RP2 from +3VSUS to +3VPCU for EC engineer suggestion Page30 : Remove 0ohm (RP7) and connect directly Page30 : Change 2.2uf to 10uf (C367)		3A	3B
				3A	3B
				3A	3B
				3A	3B
				3A	3B
				3A	3B
				3A	3B
				3A	3B
				3A	3B
				3A	3B